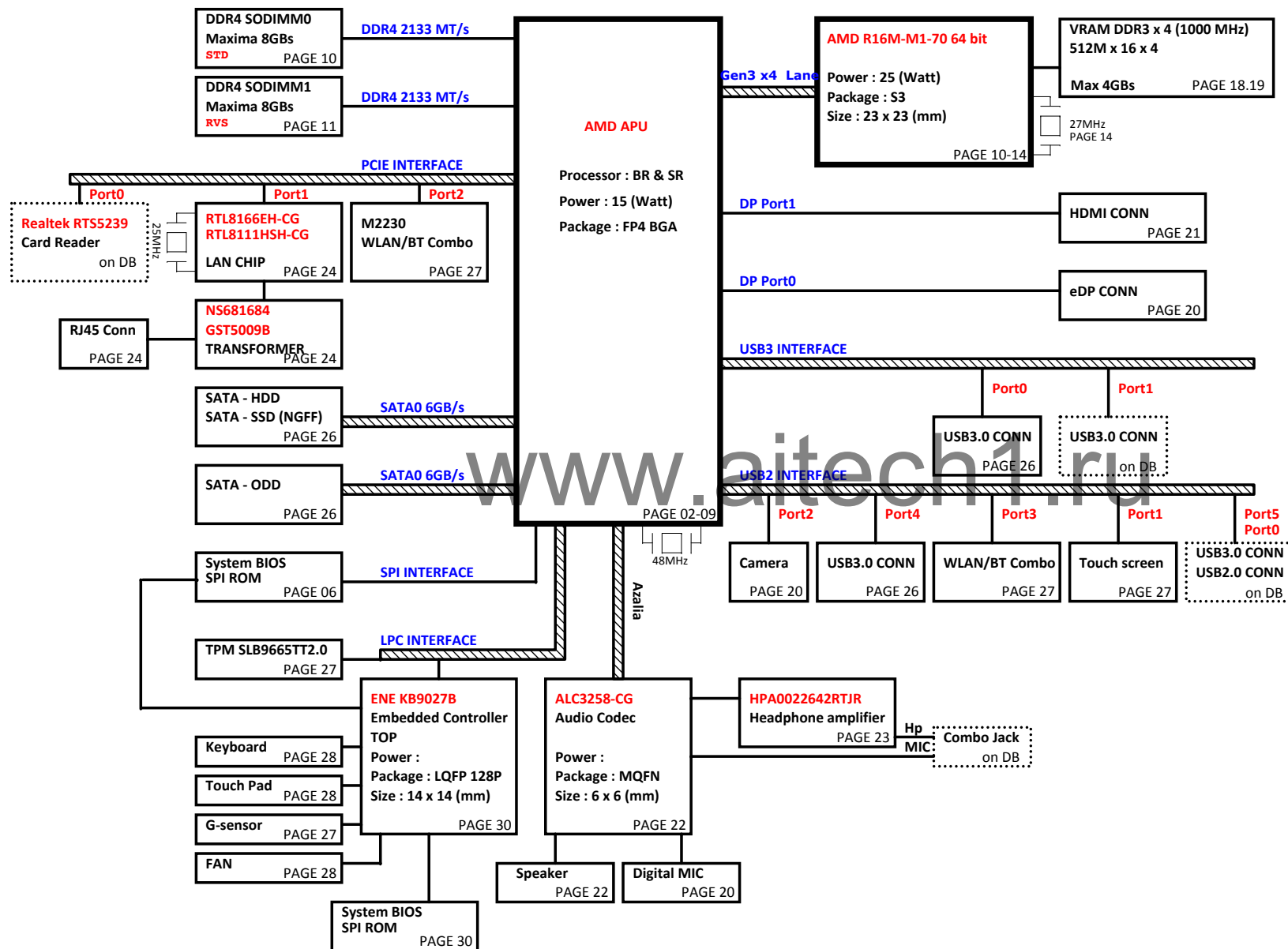


Dessert AMD BR & SR DIS/UMA 15.6"



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

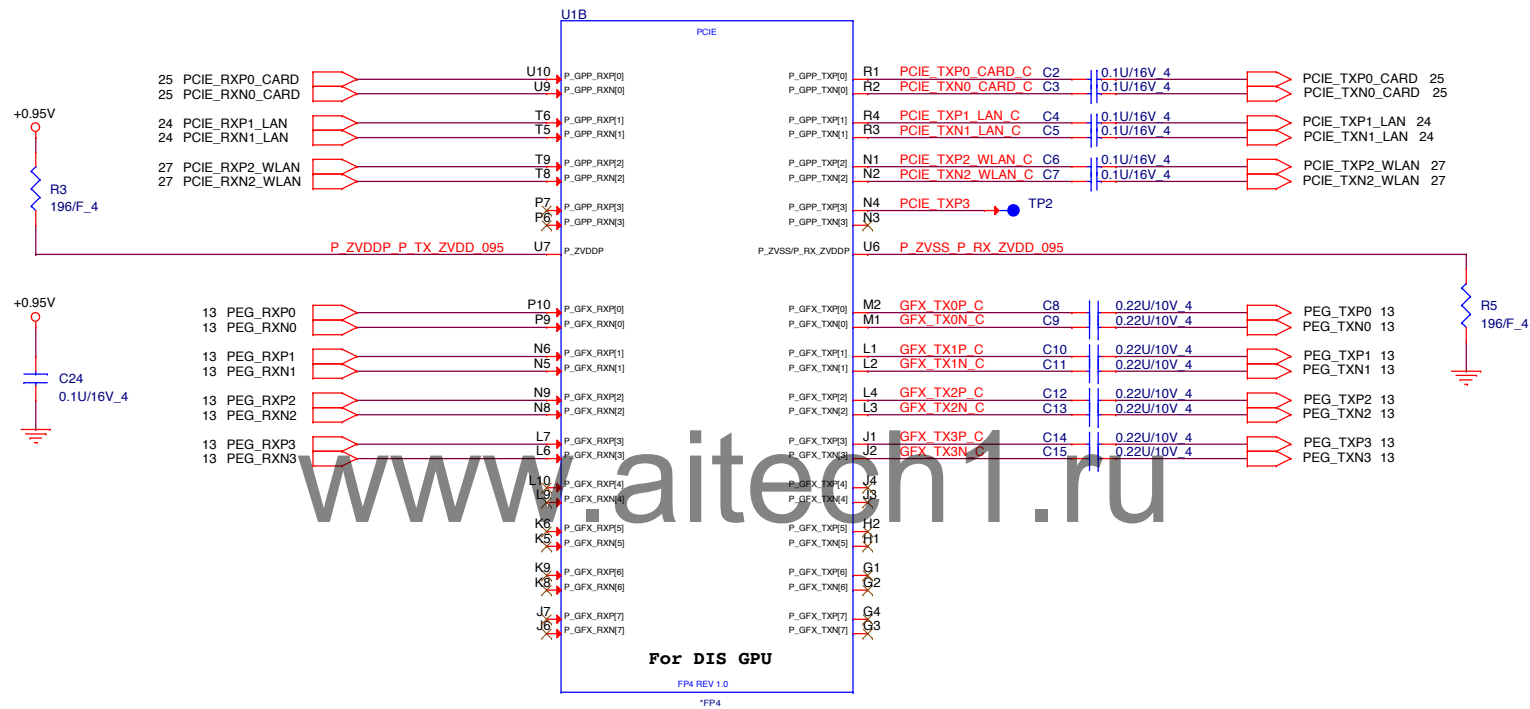
Power Source

ISL88750 System Charge Power (+BATCHG) PAGE 31
SY8208B/SY8286C System Power (+3VPCU/+5VPCU/+3VS5/+5VS5) PAGE 32
RT8231B System Memory Power (+1.2VSUS/+0.6V_DDR_VTT/+2.5VSUS) PAGE 33
APW8826/APW8826/G9336 Processor Power (+0.95VS5/1.5VS5/0.77VS5) PAGE 34
AO21267/RT8068AZQW Processor Power (+0.95V/+1.8VS5) PAGE 35
ISL62771 Processor Power (+VCC_CORE/+VDDNB_CORE) PAGE 36.37
ISL62771 Processor Power (+APU_VDDGFX) PAGE 38.39
APL3523A *3 System Power (+3/+3VLAVCC/+5V/+3VSUS/ +1.5V/+1.8V_ROM/+1.8V) PAGE 40
G5018 Processor Power (+VDDCR_FCH_S5) PAGE 41
RT3662EB/AO21236 DGPU Power (+VGA_CORE/+1.35V_VGA) PAGE 42~44
RT8068A/APL3523A DGPU Power (+0.95V_VGA/+3V_VGA/+1.8V_VGA) PAGE 45



PROJECT : G54A
Quanta Computer Inc.

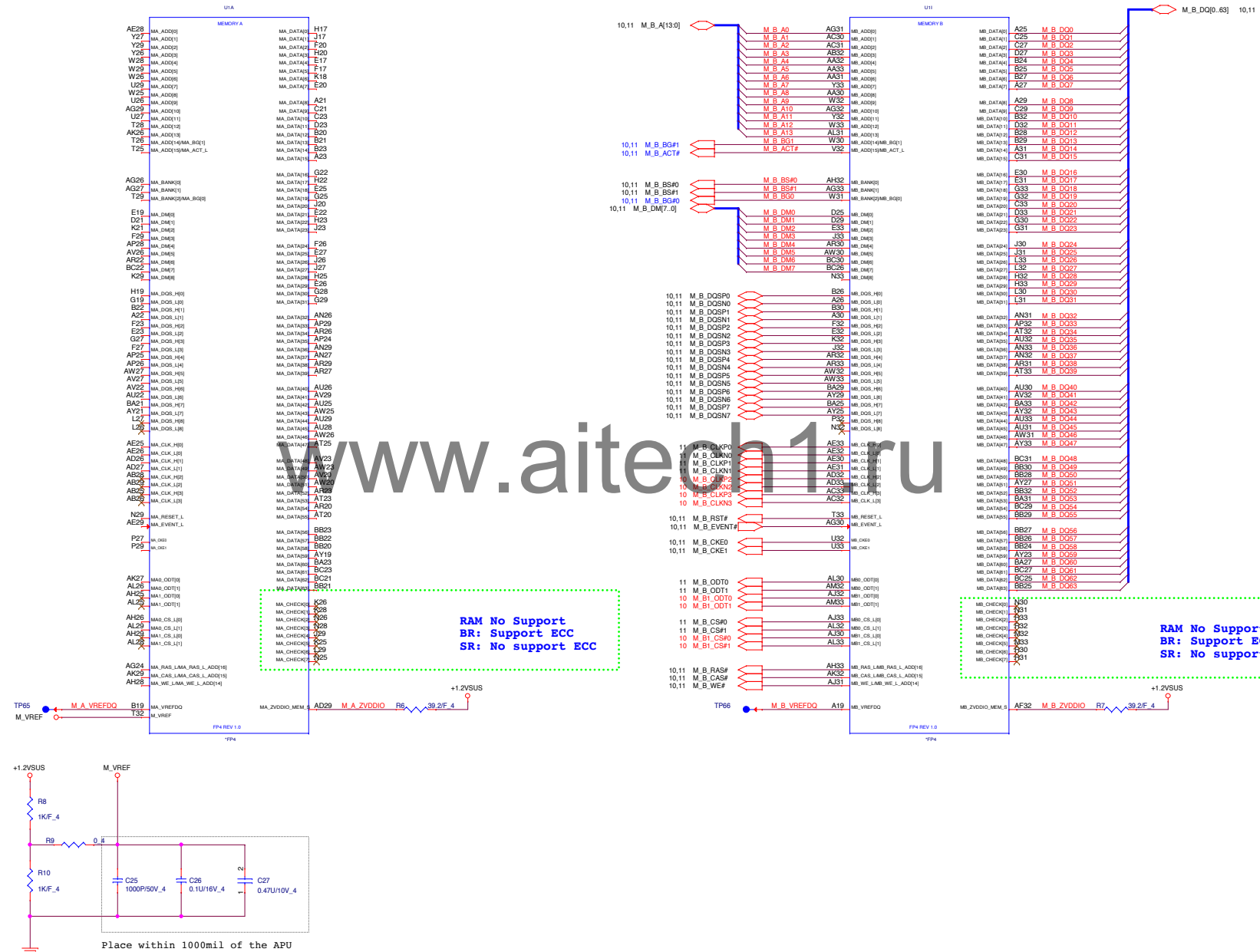
Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, January 11, 2016	Sheet	1 of 46

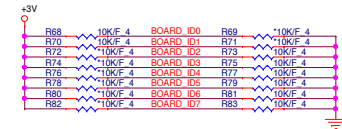
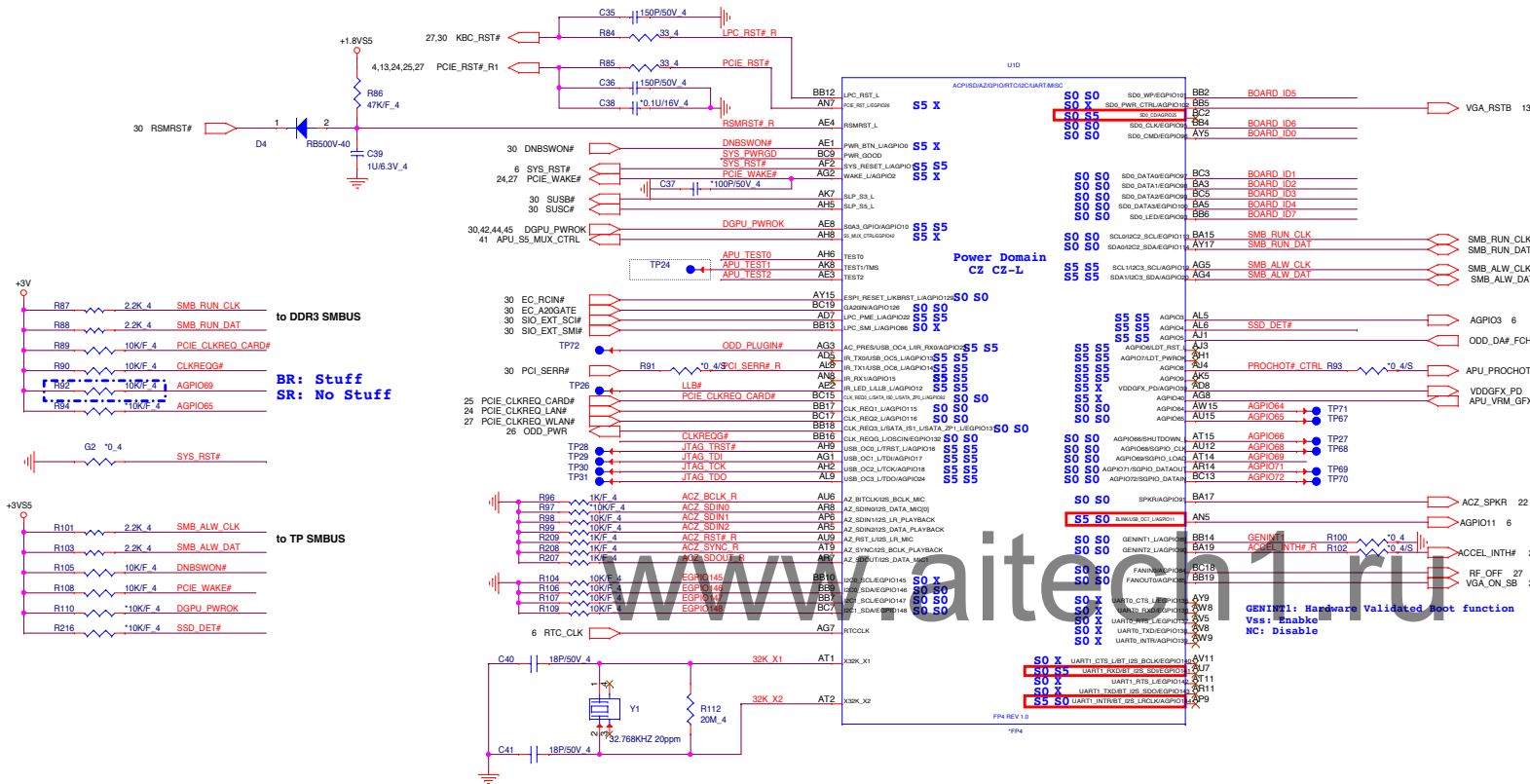


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Size	Document Number	Rev
	BR & SR 1/7(PCIE)	1A
Date: Monday, January 11, 2016	Sheet 2 of 46	

SB only channel B





BOARD ID SETTING

Board ID 0	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"
11	Reserve

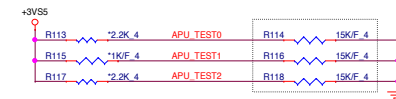
Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve
11	Reserve

Board ID [5]	Definition
0/1	BR/SR

Board ID [6]	Definition
0/1	Reserve

Board ID [7]	Definition
0/1	Reserve

Follow AMD checklist 53537_1_09 suggestion.



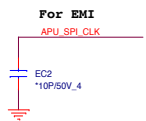
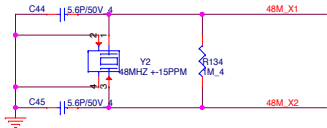
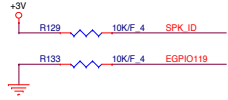
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



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Size Document Number
BR & SR 47(GPIO/AZ/UART)
Date: Monday, January 11, 2016 Sheet 5 of 46

Follow Checklist

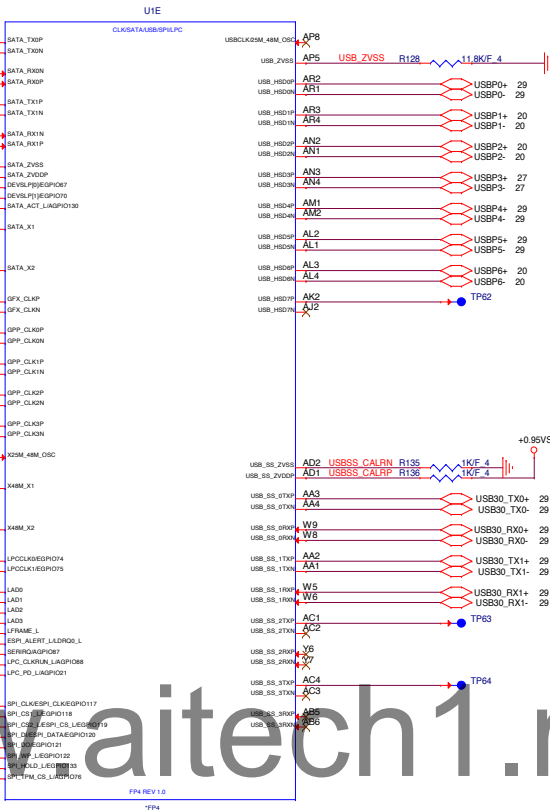
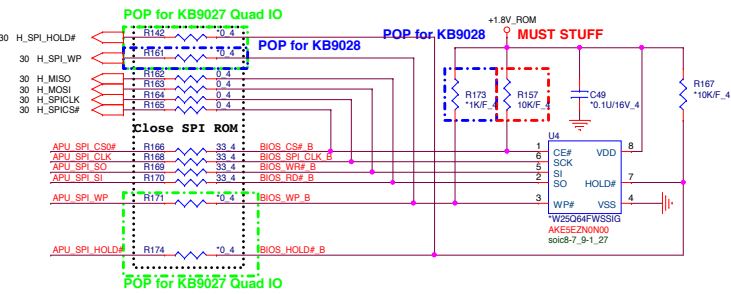
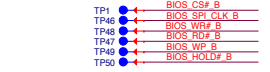


For E

APU SPI ROM

Vender	Size	P/N (1.8V)
WND	8M	AKE5EZNO00
EON	8M	AKE5EFNOQ00
	8M	
Socket	DFHS08FS023	

TPs need place to all TOP or all BO



USB2.0 CONN ON DB

TOUCH SCREEN

CAMERA

BT

USB3.0 CONN ON MB

USB3.0 CONN ON DB

IR CAM

USB2 & USB3 MAPPING (Use form Port4)
 USB2 PORT4 -> USB3 PORT0

```
USB2  PORT4 => USB3  PORT0
USB2  PORT5 => USB3  PORT1
```

```
USB2  PORT5 => USB3  PORT1
USB2  PORT6 => USB3  PORT2
```

```
USB2  PORT6 => USB3  PORT2
USB2  PORT7 => USB3  PORT3
```

Support S3-S5 wake up

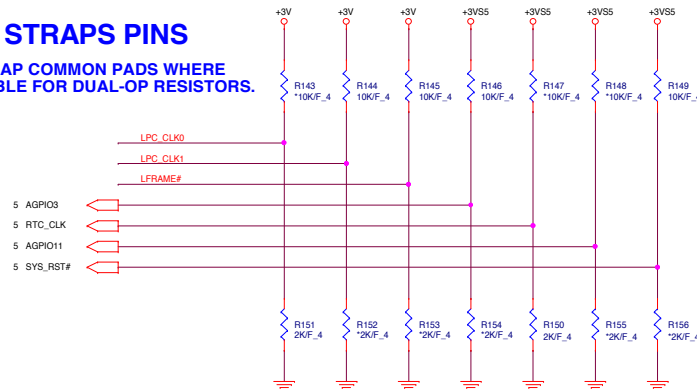
29 **USB3.0 CONN ON ME**
30

29 **USB3.0 CONN ON DE**
30



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

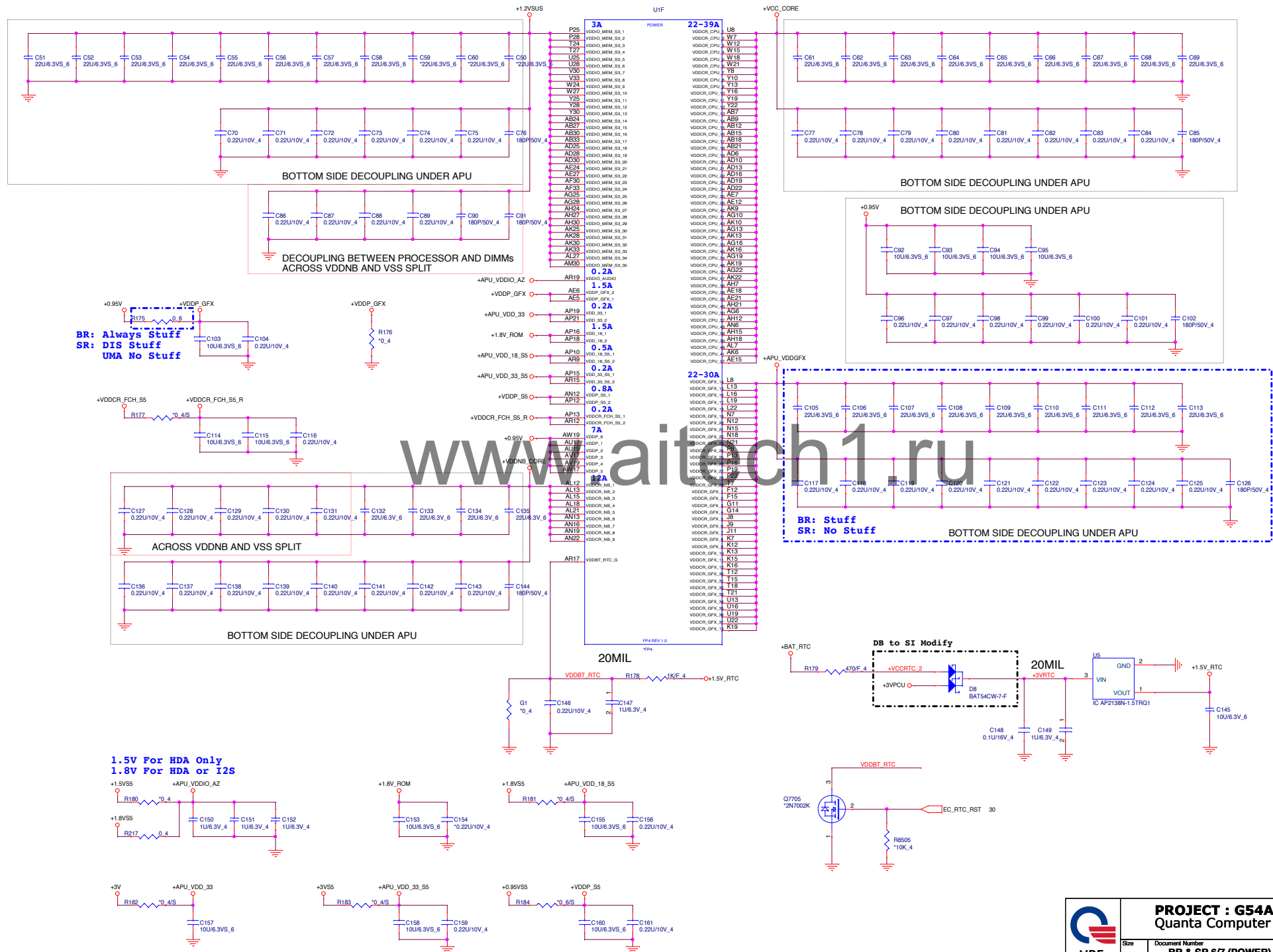


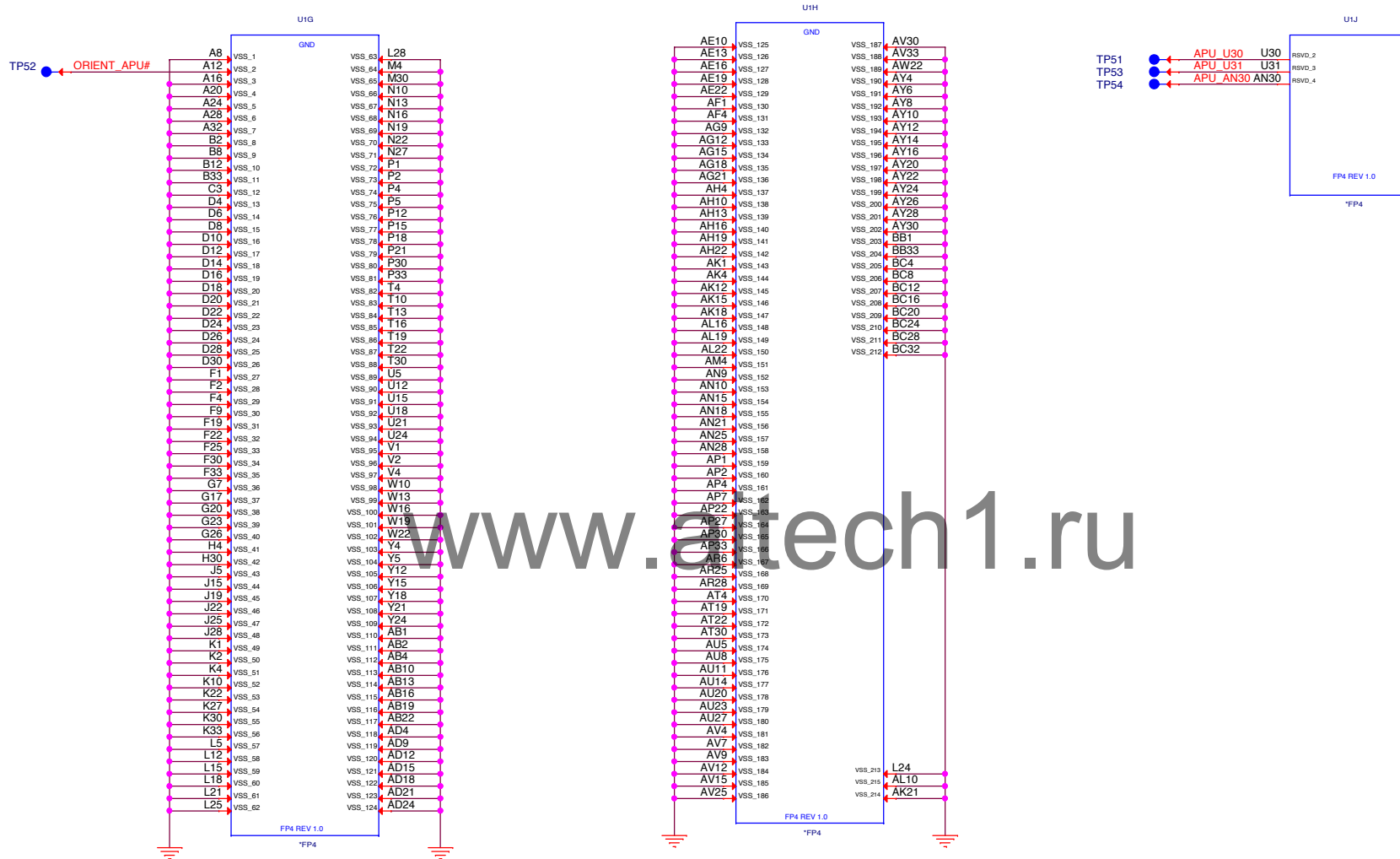
REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3	RTC_CLK	AGPIO11=BLINK	SYS_RST#
				Q2-L SR Pull-Up SR & SR	Int PWRGD Int PWRGD	Int Pull-Up Int PWRGD	
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks	SPI ROM DEFAULT	1.8V SPI ROM Enhanced reset logic (for quicker SS resume) DEFAULT	Coin battery is not on board. DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM DEFAULT	Coin battery is not on board. DEFAULT	LDT_RST#/LDT_PWRGD output to Pads	short reset mode DEFAULT



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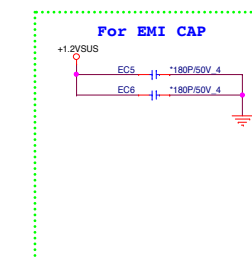


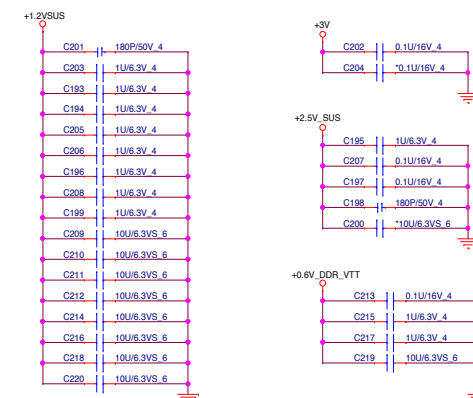
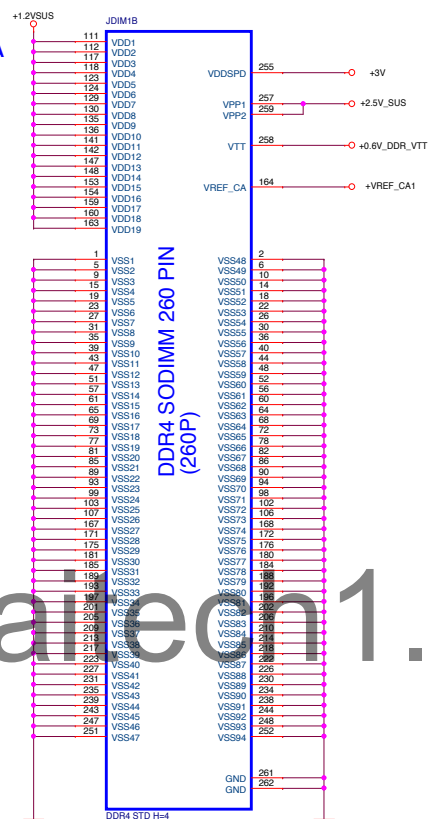
PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	BR & SR 7/7 (GND)	1A
Date: Monday, January 11, 2016	Sheet 8 of 46	

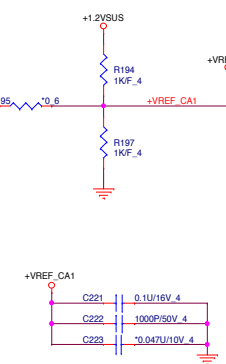
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www.aitech1.ru

 NB5	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, January 11, 2016 Sheet 9 of 46		

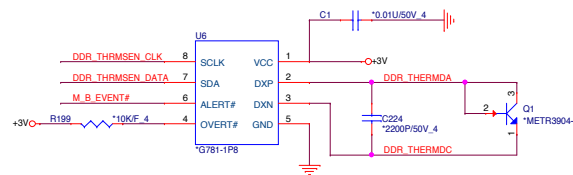
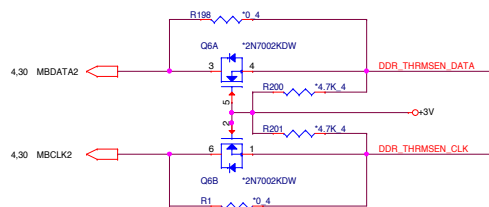




1uF/10uF 4pcs on each side of SODIMM




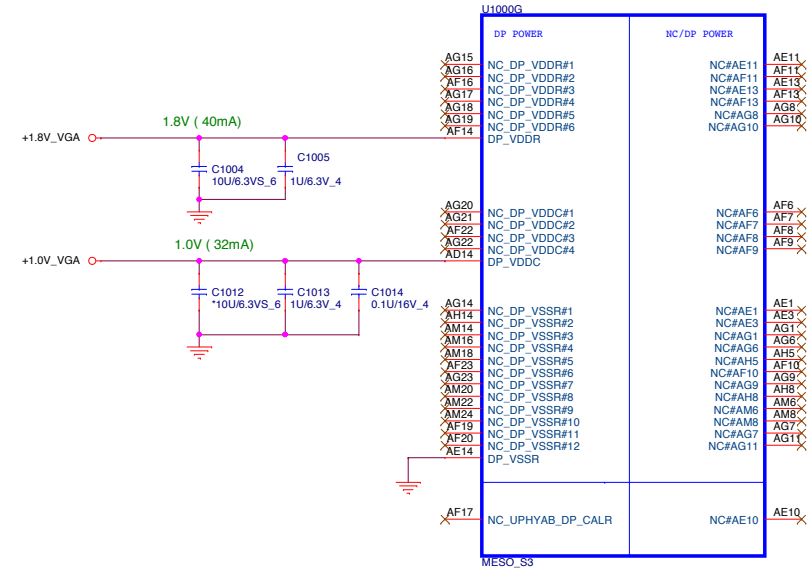
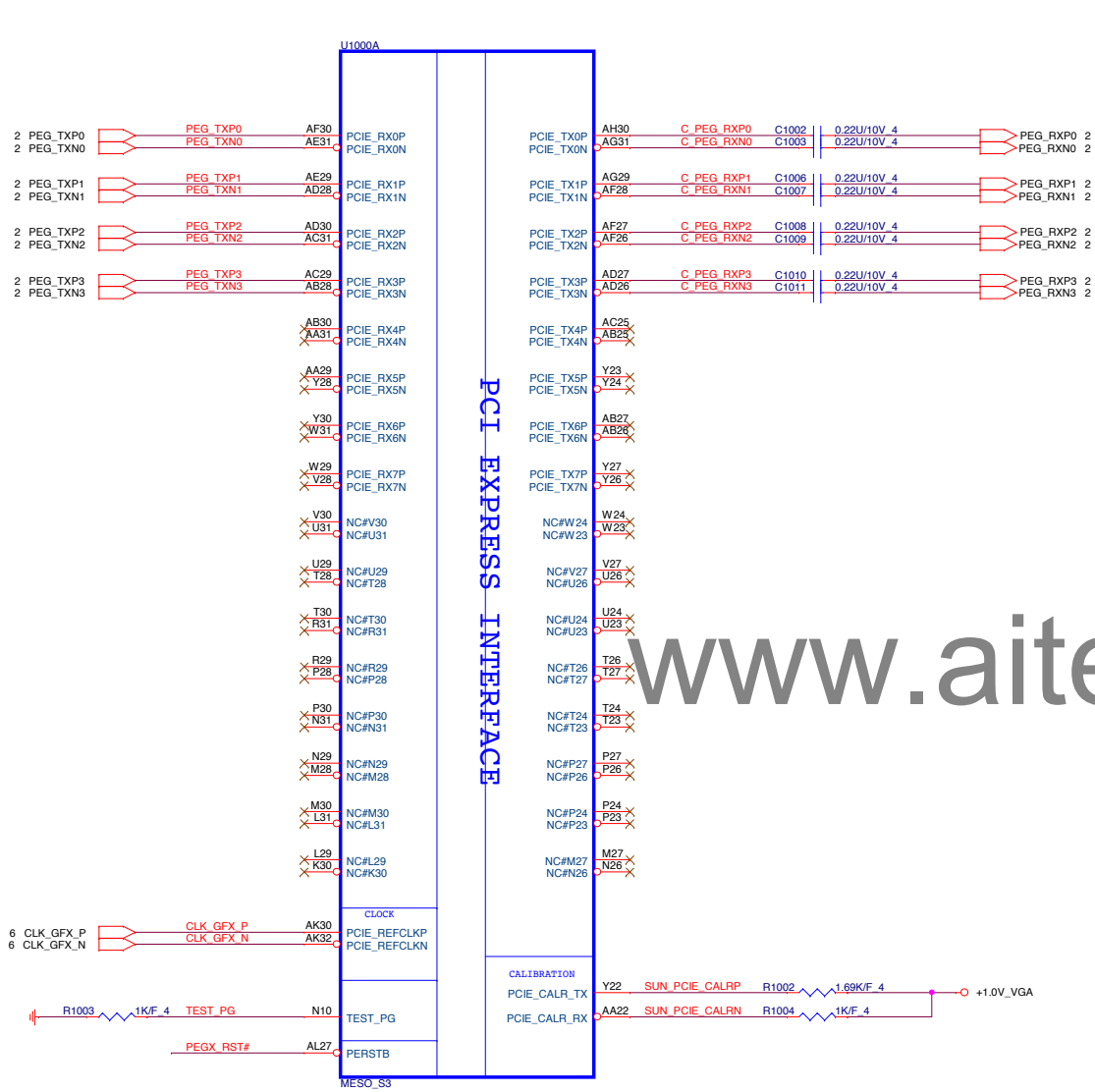
For EMI CAP



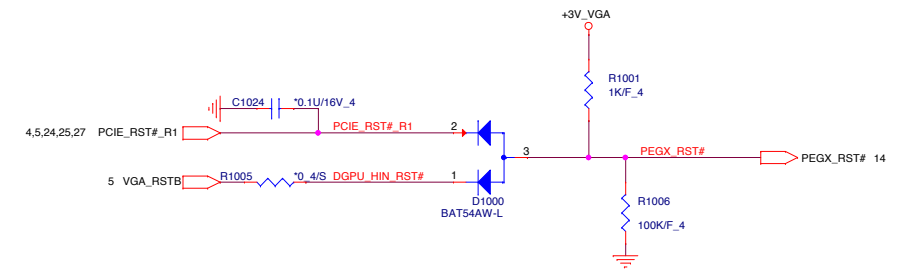
Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

<Reserved for CHB – DIMM2>
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 NB5	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number CHB DDR4 DIMM2-RVS(4.0H)	Rev 1A
	Date: Monday, January 11, 2016 Sheet 12 of 46		



GPU Reset Signal



PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_PCIE/DP POWER	1A
Date: Monday, January 11, 2016	Sheet	13 of 46

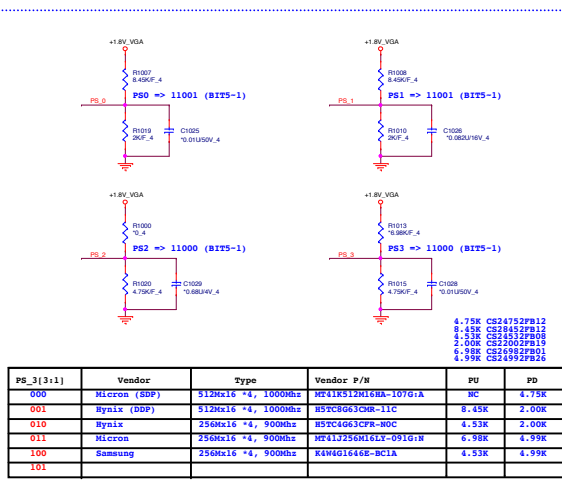
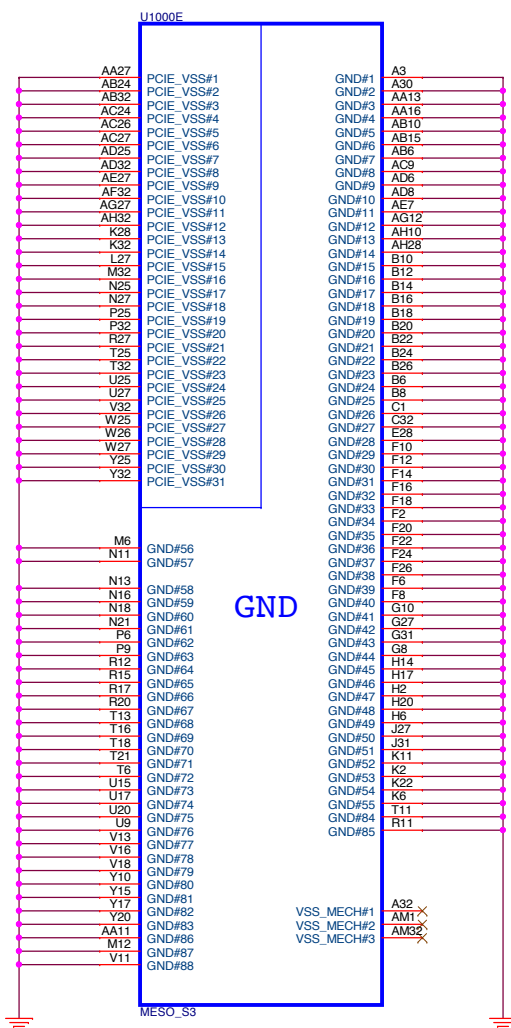


Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0101	RON_CFG0010	If STRAP_BIOS_ROM_EN = 1 RON_CFG0010 defines the ROM version.	Design dependent, see the description.
PS_0102	RON_CFG0011	If STRAP_BIOS_ROM_EN = 1 RON_CFG0011 defines the primary memory aperture size. See <i>Sanituary Memory Aperture Size</i> (p. 29).	Design dependent, see the description.
PS_0103	RON_CFG0012		
PS_0104	N/A	Reserved for internal use only. Start bit 1 at set.	1
PS_0105	N/A	Reserved.	1
PS_1101	STRAP_BIOS_GEN_EN_A	1 = PCIE BIOS capability. 0 = PCIE BIOS is supported. Determine whether or not the PCIE reference clock power management capability is supported in the T10 configuration space (see <i>Power Management</i> in <i>CLARIFAR</i>). 0 = The CLARIFAR power management capability is disabled. 1 = The CLARIFAR power management capability is enabled.	Design dependent, see the description.
PS_1102	STRAP_BIF_CLK_P0_EN	Reserved for internal use only. Start bit 0 at set.	0
PS_1103	N/A	Reserved.	0
PS_1104	STRAP_TX_CFG_OVR_PULL_DOWN	0 = The transmitter full-half swing mode. 1 = The transmitter full-half swing is enabled.	1
PS_1105	N/A	Reserved.	1
PS_1106	STRAP_TX_GREENPH_EN	PCI EXPRESS® transmitter-disable enable. 0 = Tx despreads disabled. 1 = Tx despreads enabled.	Design dependent, see the description.
PS_2101	N/A	Reserved.	0
PS_2102	N/A	Reserved.	0
PS_2103	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2104	N/A	Reserved.	1
PS_2105	N/A	Reserved.	1
PS_3101	BOARD_CFG0010	Board configuration-related information such as for memory ID.	Design dependent, see the description.
PS_3102	BOARD_CFG0011		
PS_3103	BOARD_CFG0012		
PS_3104	N/A	Reserved.	1
PS_3105	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS **ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,** **THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

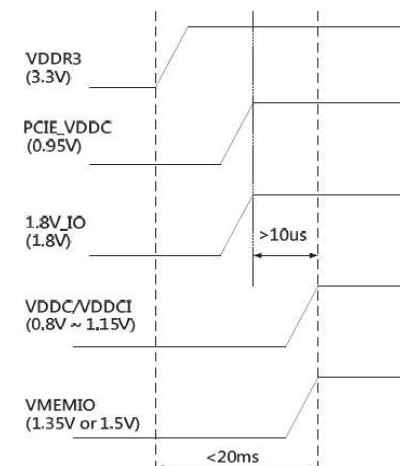
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

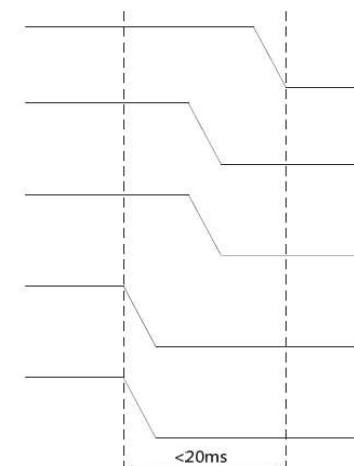
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

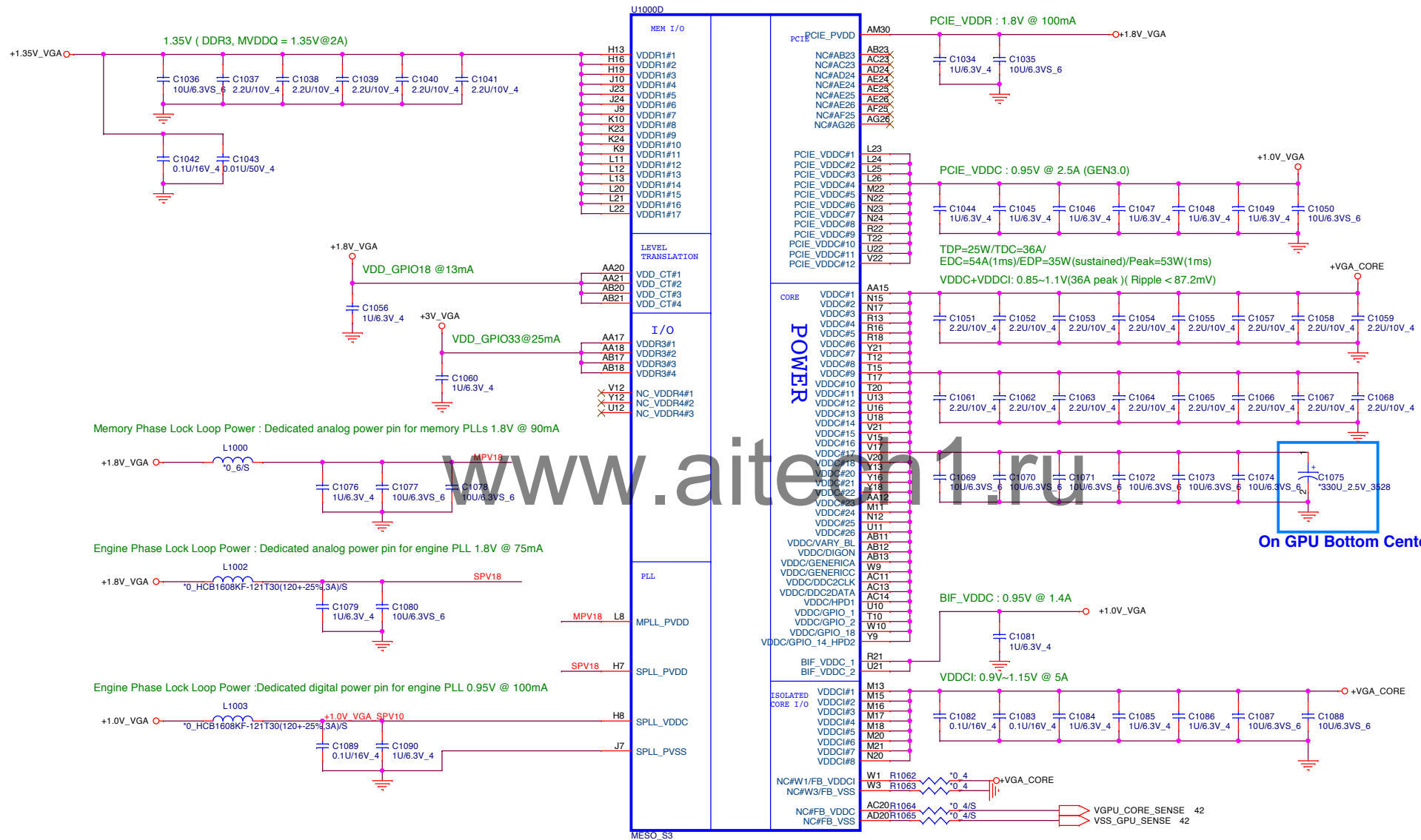


POWER DOWN



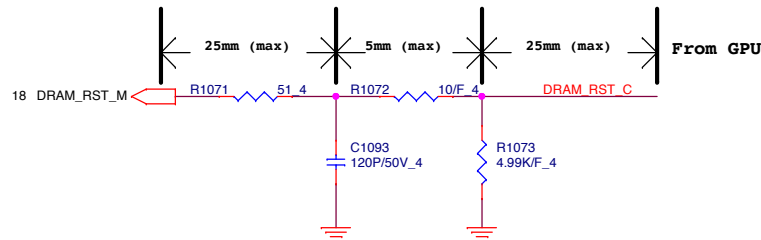
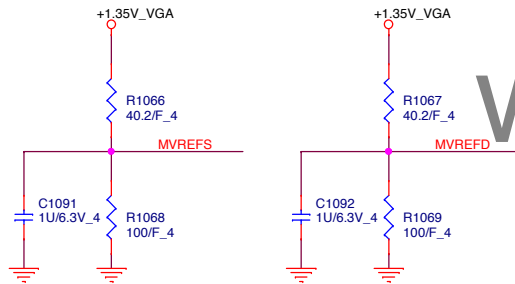
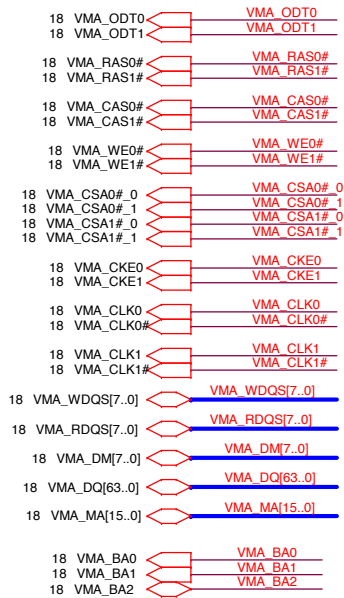
PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
M1-70_S3_GND/LVDS/Strap	1A	
Date: Monday, January 11, 2016	Sheet 15 of 46	



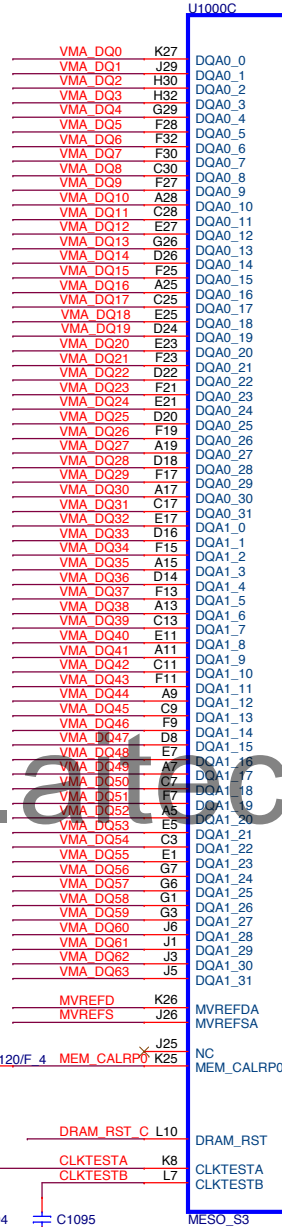
PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_POWER	1A
Date:	Monday, January 11, 2016	Sheet 16 of 46

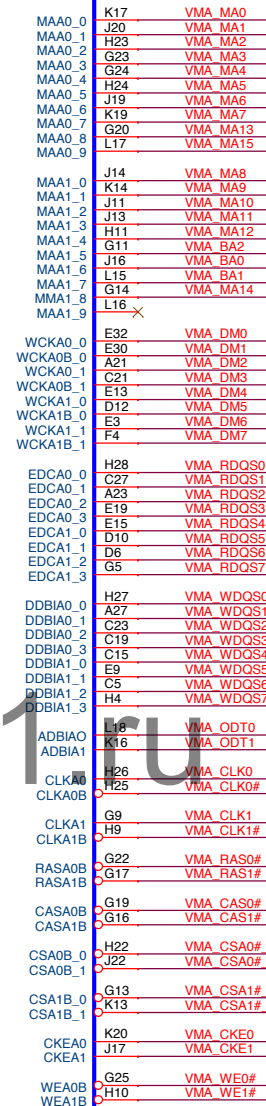


Place all these components very close to GPU. (Within 25mm)
Keep all component close to each Other. (within 5mm)

This basic topology should be used for DRAM_RST for DDR3/GDDR5.

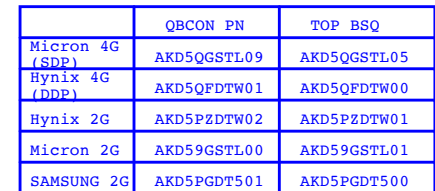


MEMORY INTERFACE




PROJECT : G54A
Quanta Computer Inc.

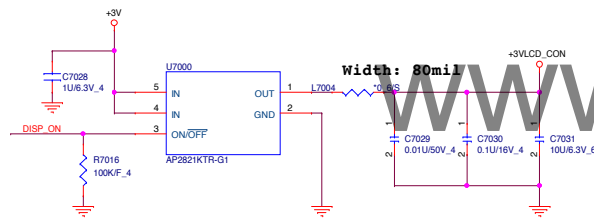
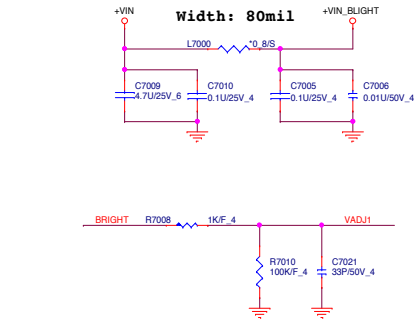
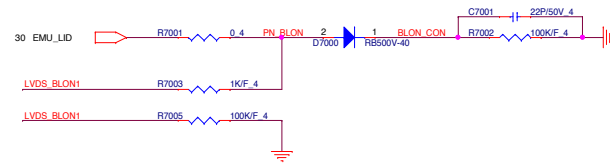
Size	Document Number	Rev
	M1-70_S3_MEM	1A
Date:	Monday, January 11, 2016	Sheet 17 of 46



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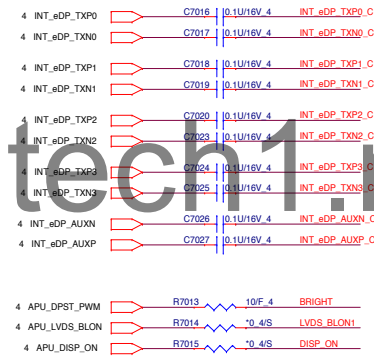
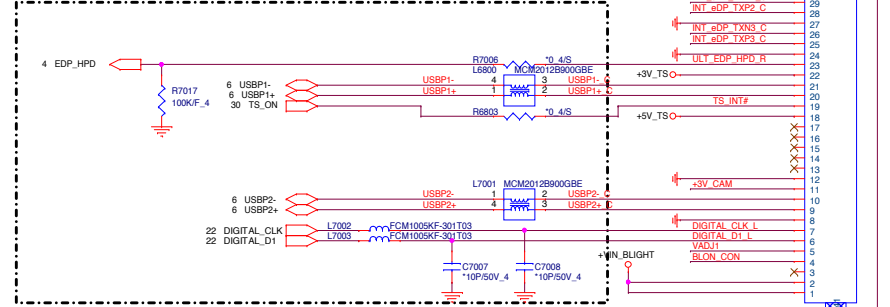
 NB5	PROJECT : G54A		
	Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
Date: Monday, January 11, 2016		Sheet 19 of 46	

LID Switch

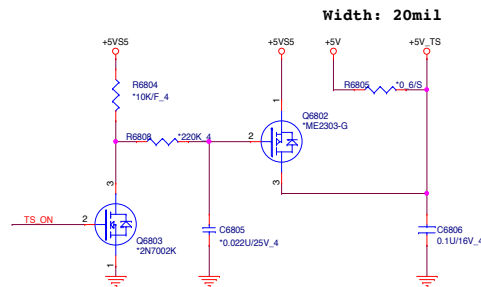
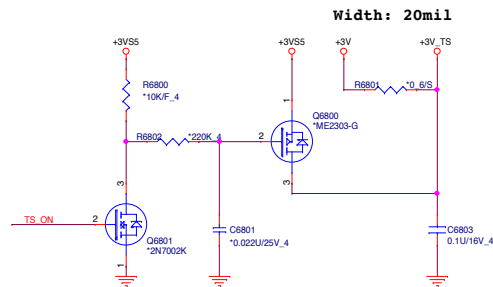


eDP CONN.

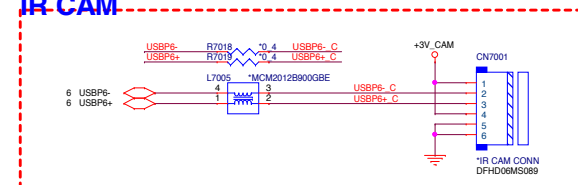
DB to SI Modify

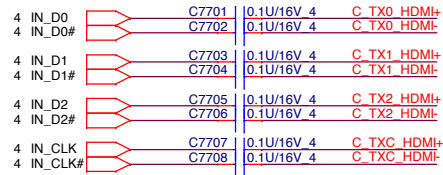


Touch screen

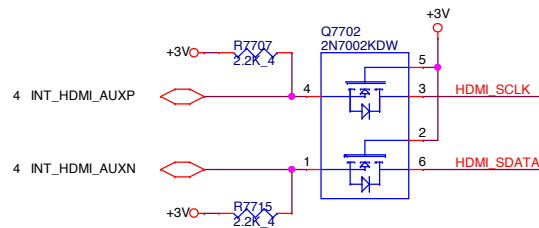


IR CAM



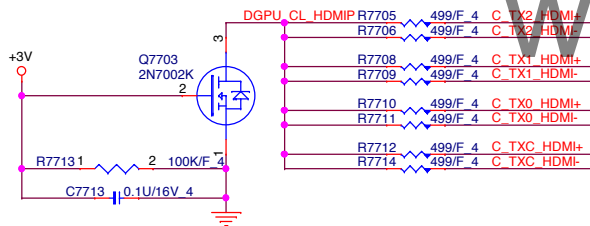
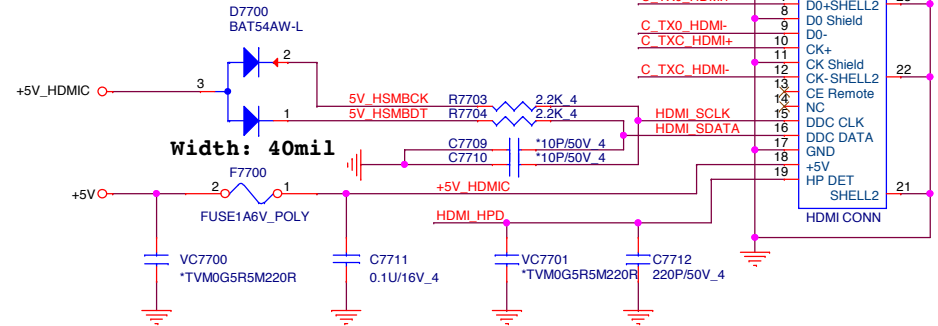


HDMI SMBus Isolation

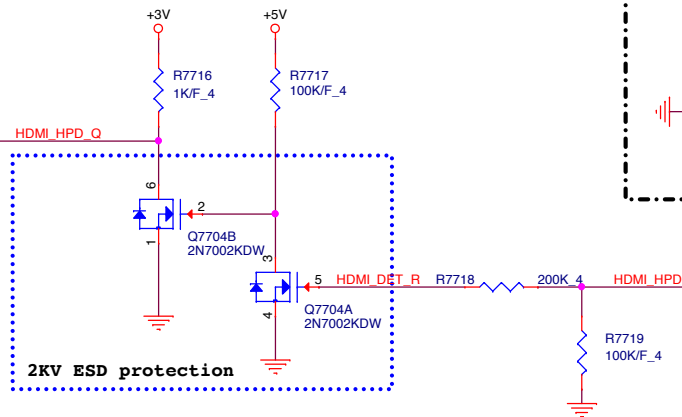


DB to SI Modify

For EMI

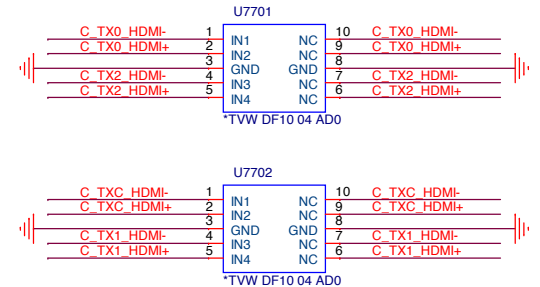


4 HDMI_HPD_Q



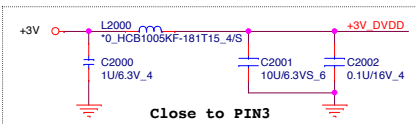
2KV ESD protection

DB to SI Modify

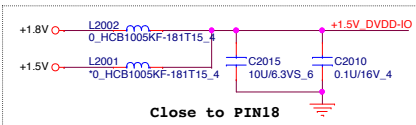


PROJECT : G54A
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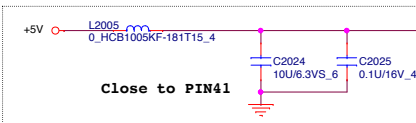
Size	Document Number	Rev
B	HDMI CONN	1A
Date:	Monday, January 11, 2016	Sheet 21 of 46



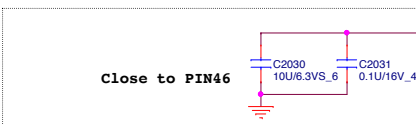
30mA



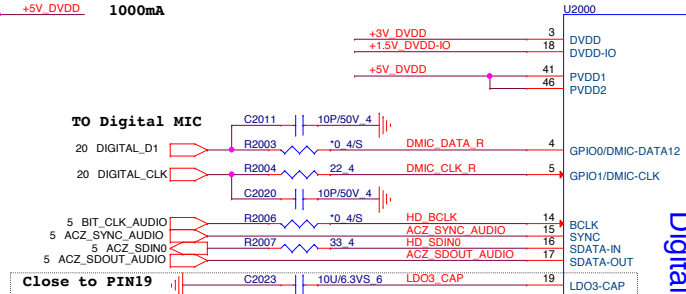
10mA



1000mA

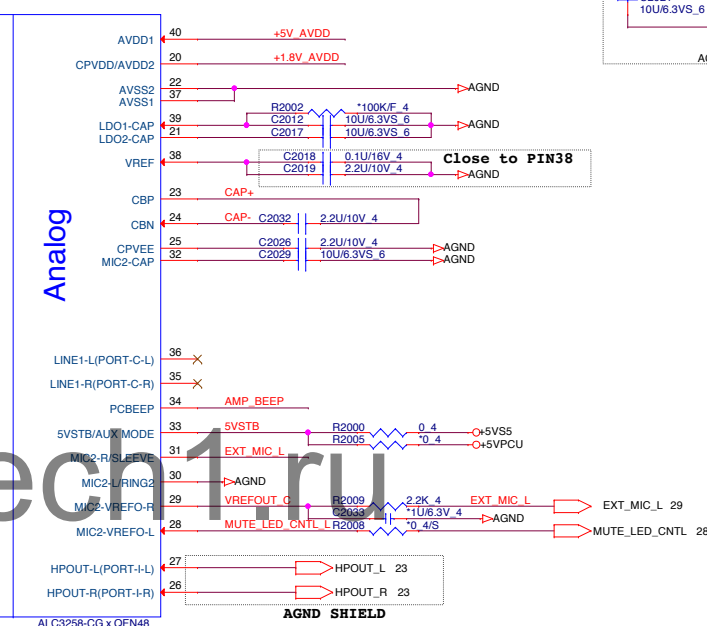


Close to PIN46



TO Digital MIC

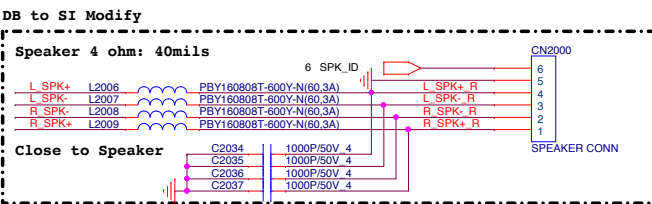
Close to PIN19



Digital

Analog

ALC3258-CG x QFN48

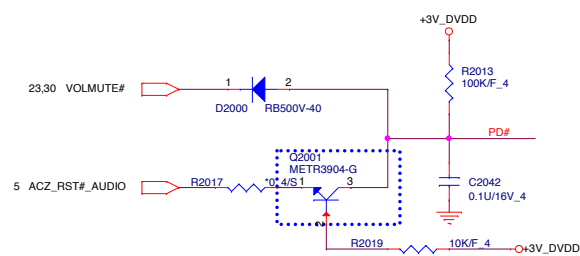


DB to SI Modifv

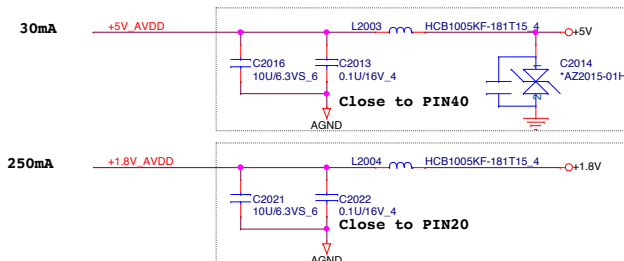
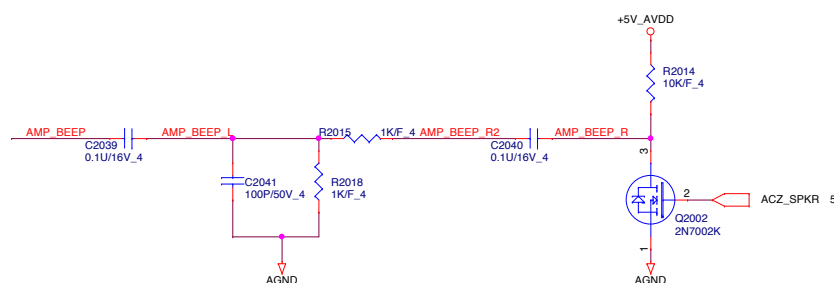
Speaker 4 ohm: 40mils

- **Close to Speaker**

Speaker 4 ohm: 40mils



No Stuff: If HP need beep sound when RST# at low state.

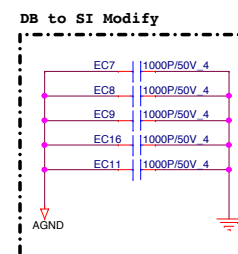


30mA

+5V_AVDD

Close to PTN40

Close to PIN20

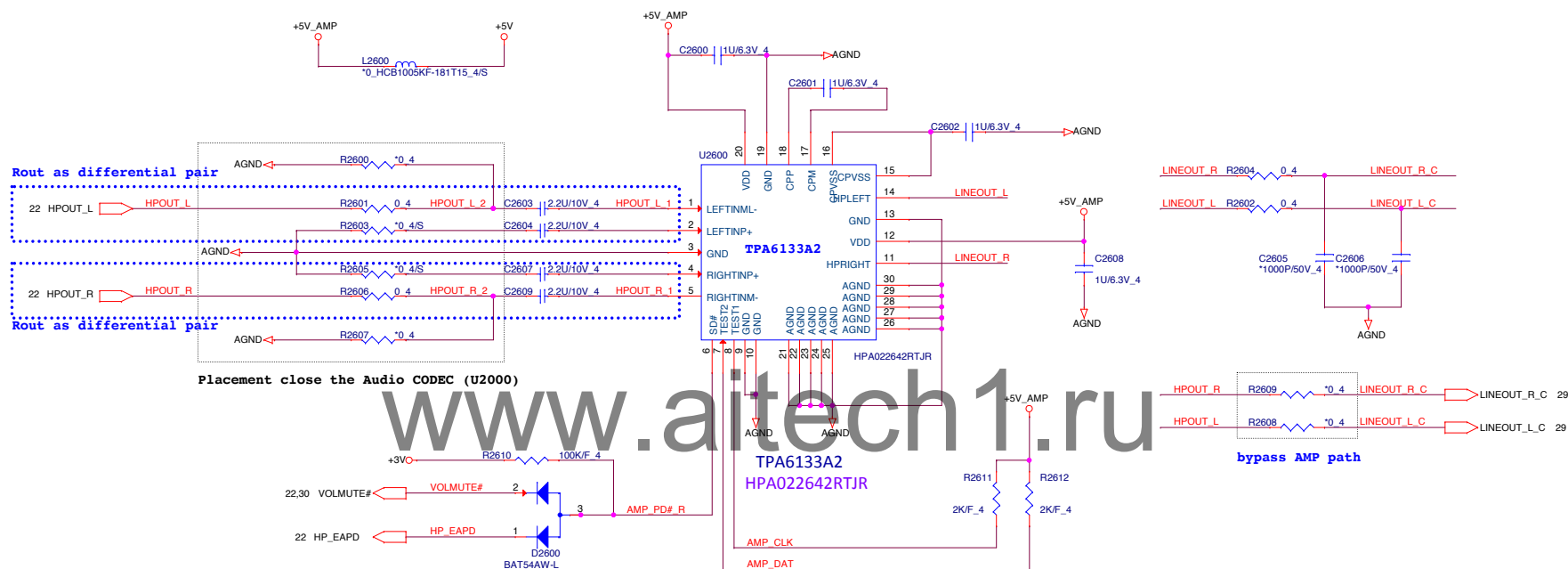


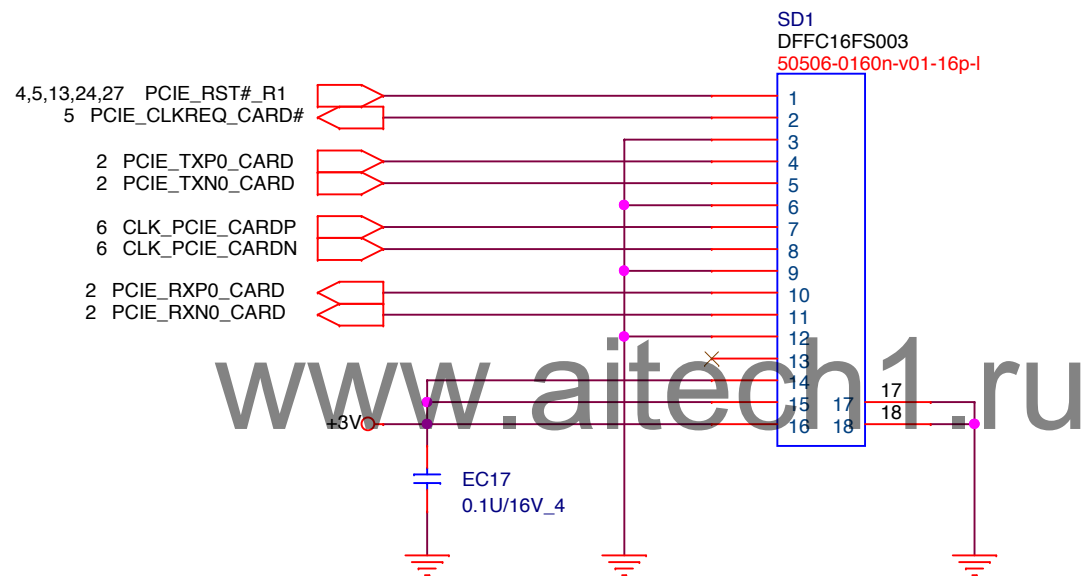
DB to SI Modifv

place to near or under codec

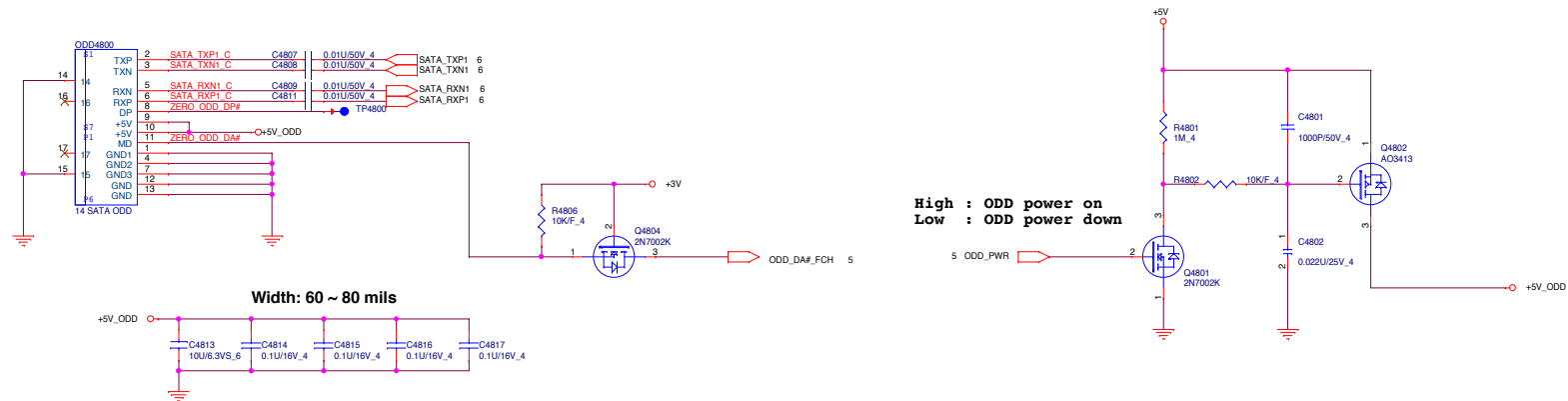


Head Phone Out





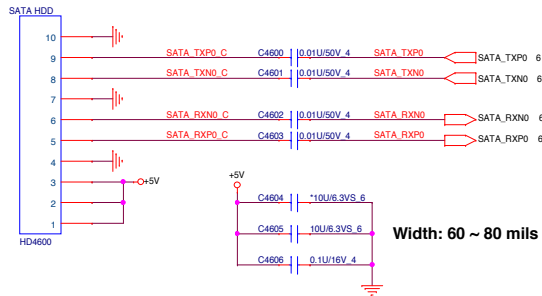
SATA ODD



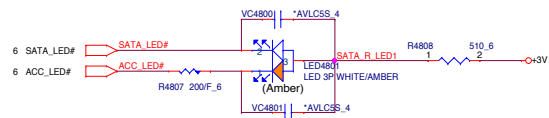
SATA HDD

SATA SSD

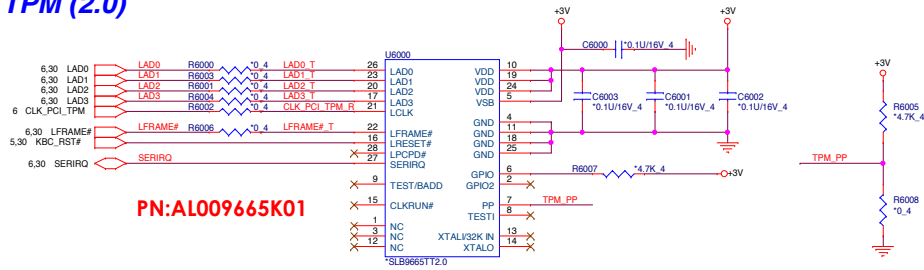
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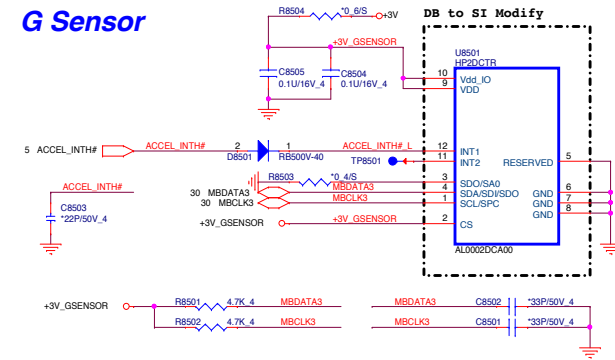
SATA LED



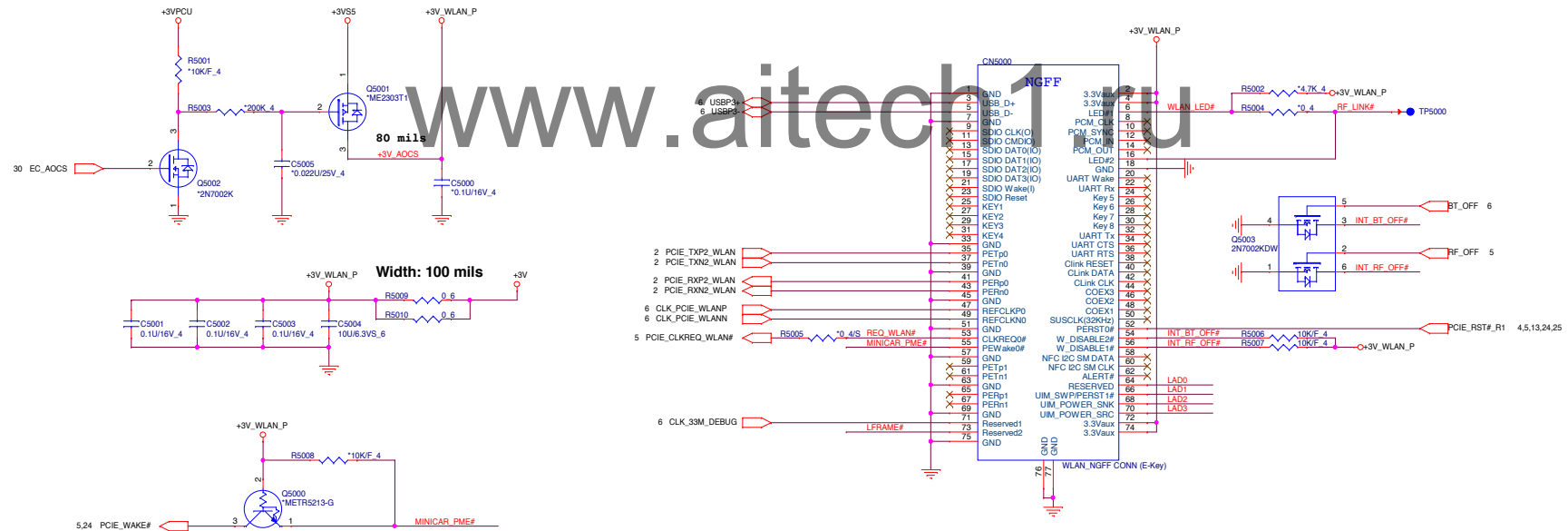
TPM (2.0)



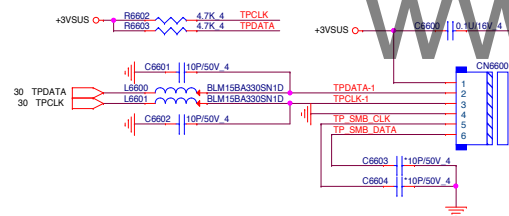
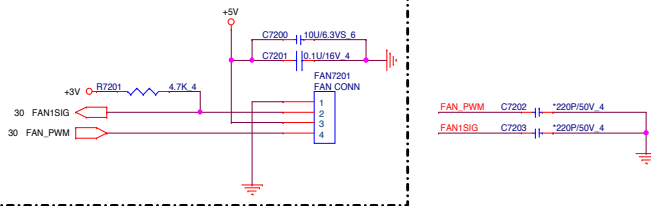
G Sensor



WLAN & BT



FAN CONN.



30 NBSWON1#

29,46 LID#

30 DEEP_PWLED#

EC18 *220P/50V_4

EC19 *220P/50V_4

EC20 *220P/50V_4

+BAT_RTC

+3VPCU

CN7900 POWER CONN

Pin1 : NBSWON1#

Pin2 : GND

Pin3 : LID#

Pin4 : +BAT_RTC(LIDSWITCH PWR)

Pin5 : DEEP_PWLED#

Pin6 : +3VPCU(LED PWR)

+3VPCU

+BAT_RTC

C7901 0.1uH/16V_4

C7902 0.1uH/16V_4

[illegible]

MY6	C6500	220P/50V 4
MY6	C6501	220P/50V 4
MY3	C6502	220P/50V 4
MY7	C6503	220P/50V 4
MY8	C6504	220P/50V 4
MY5	C6505	220P/50V 4
MY10	C6506	220P/50V 4
MY11	C6507	220P/50V 4
MY1	C6508	220P/50V 4
MY2	C6509	220P/50V 4
MY4	C6510	220P/50V 4
MY0	C6511	220P/50V 4
MX4	C6512	220P/50V 4
MX6	C6513	220P/50V 4
MX3	C6514	220P/50V 4
MX2	C6515	220P/50V 4
MX0	C6516	220P/50V 4
MX7	C6517	220P/50V 4
MX5	C6518	220P/50V 4
MX1	C6519	220P/50V 4
MY12	C6520	220P/50V 4
MY13	C6521	220P/50V 4
MY14	C6522	220P/50V 4
MY15	C6523	220P/50V 4
MY16	C6524	220P/50V 4
MY17	C6525	220P/50V 4

30 KB_LED_ENF

+VIN

R6509 1M_4

Q6504 2N7002K

Q6503 PMV30UN2

R6510 2M_4

+5V

Width: 20 ~ 30 mils

+5V LED_KB_LIGHT

C6526 0.1U/16V_4

C6527 0.1U/16V_4

KB_LIGHT_CONN

CN8501

4

3

2

1

DC_JACK
90W

Place this ZVS close to
Diode away +VIN

Do Not add test pad on BATDIS_G signal

+BAT_RTC

31 2S1P 41Wh

Place this cap
close to EC

6V 15A

Place this cap
close to EC

Place this cap
close to EC

Place this cap
close to EC

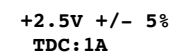
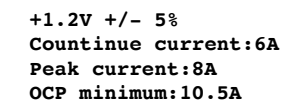
Fsw=614KHz

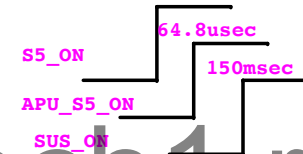
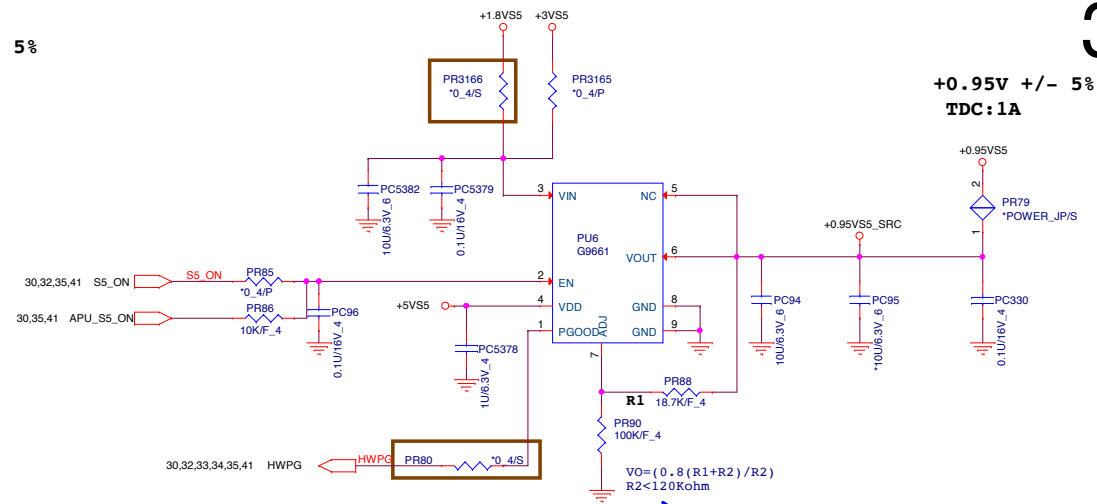
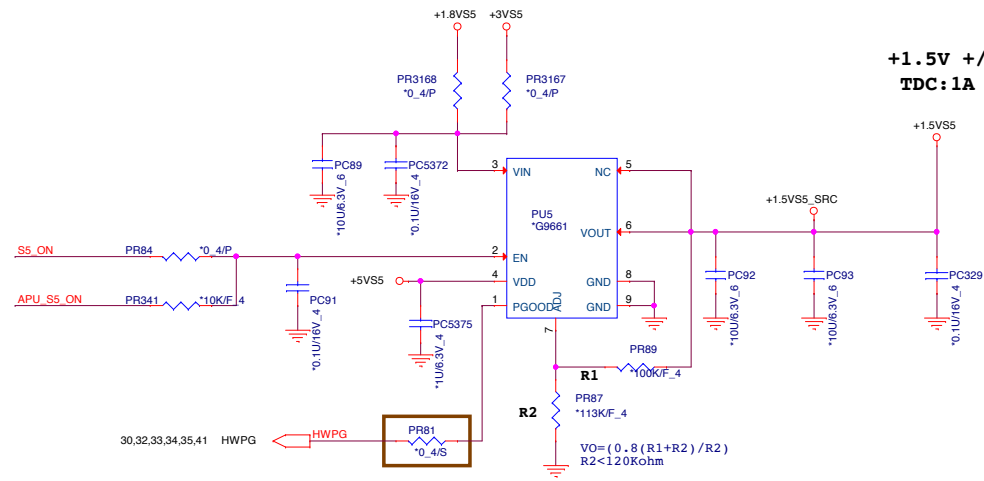
default setting 2S battery and NVDC



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL88750)	1A
Date: Monday, January 11, 2016		Sheet 31 of 46

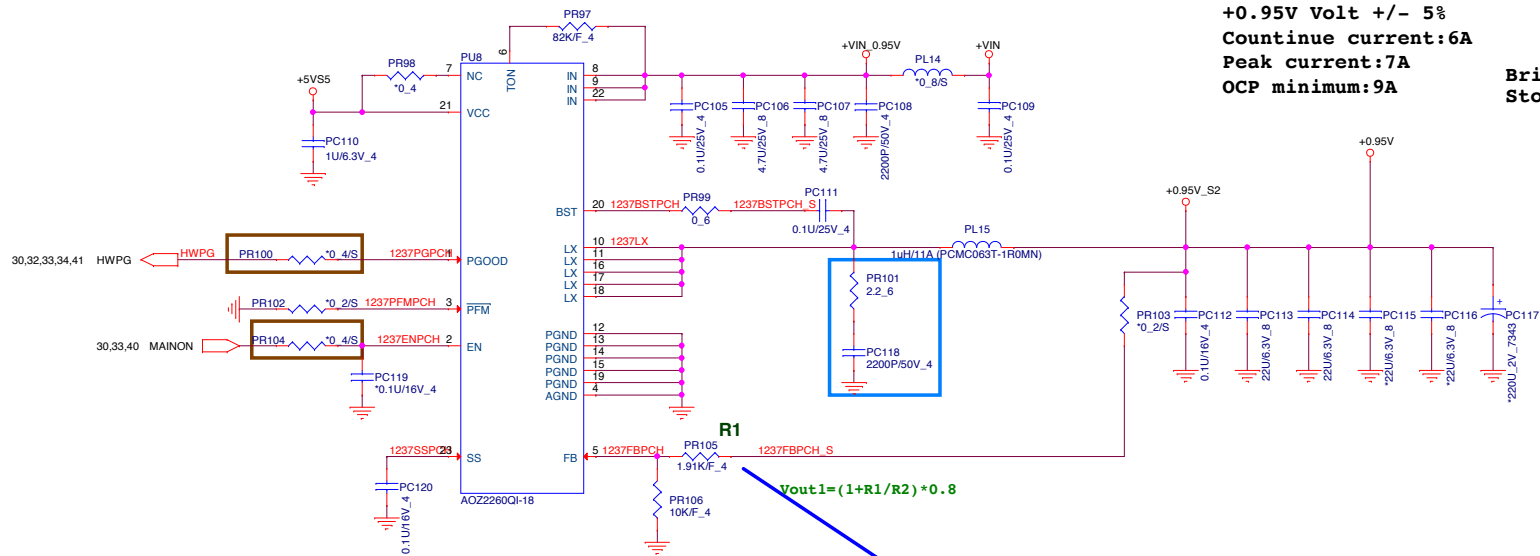




	R1		
	R1		
Stoney	18.7K	CS31872FB19	0.95V
Bristol	31.6K	CS33162FB14	1.05V

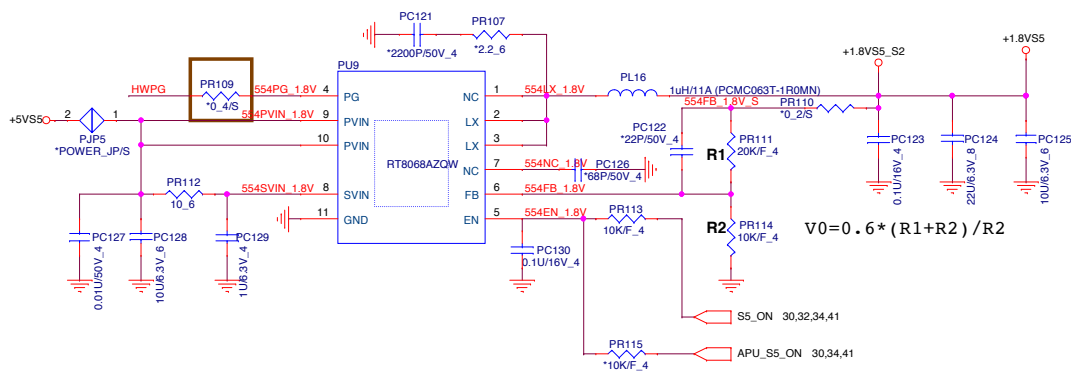
Bristol VDDP=1.05V
Stoney VDDP=0.95V

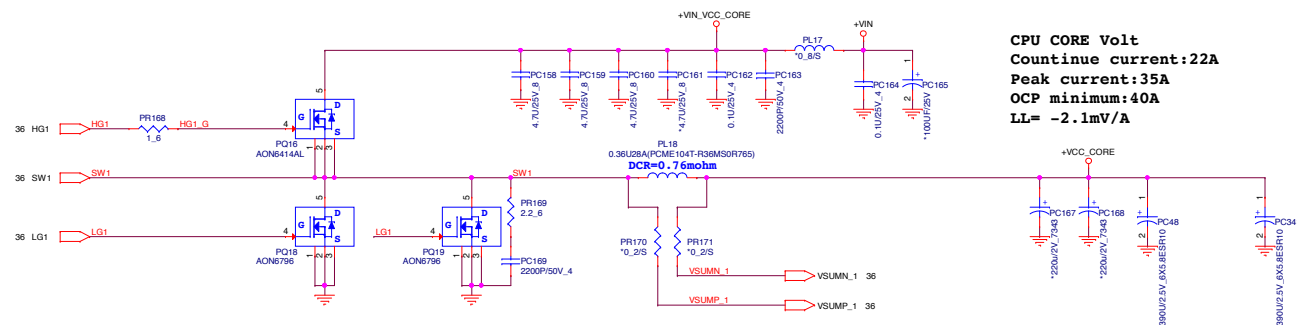
www.aitech1.ru



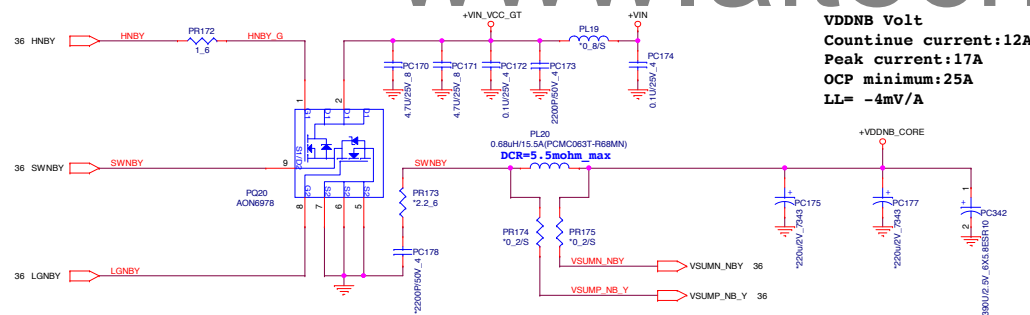
	R1		
Stoney	1.91K	CS21912FB13	0.95V
Bristol	3.16K	CS23162FB04	1.05V

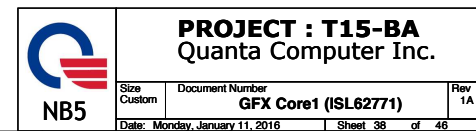
1.8VS5 +/- 3%
TDC: 3A
EDP: 4A

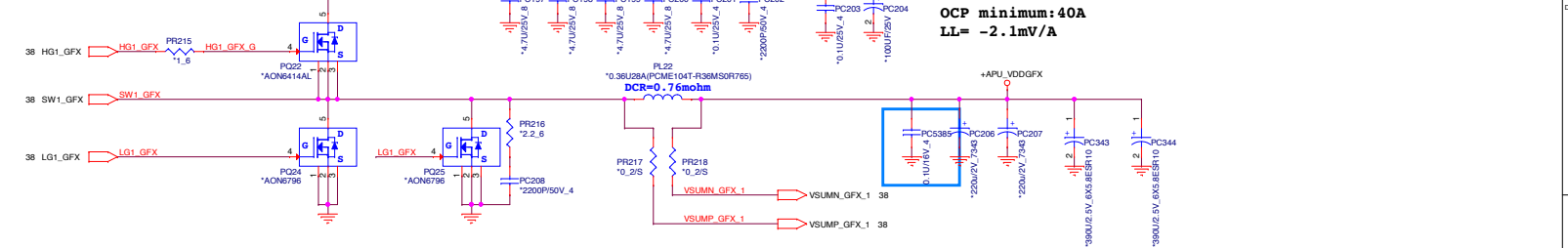




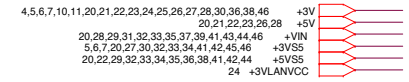
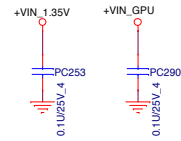
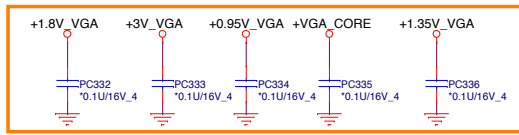
www.aitech1.ru



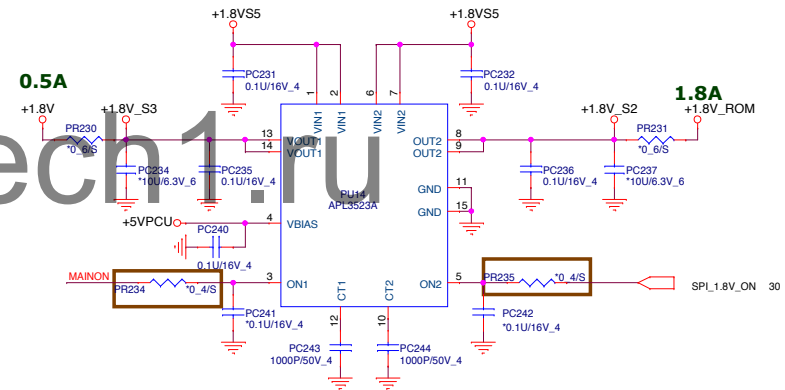
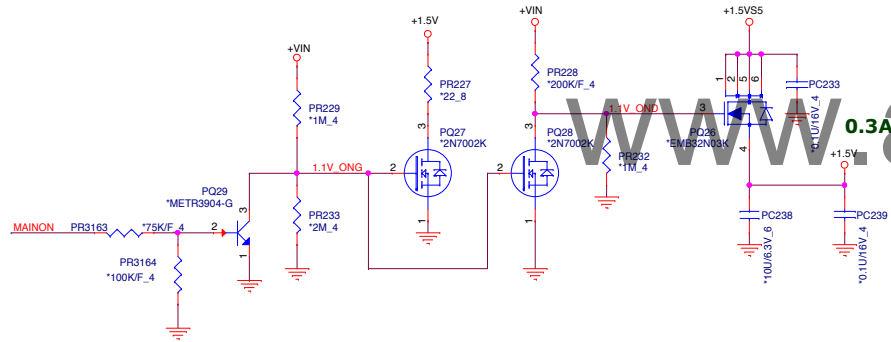
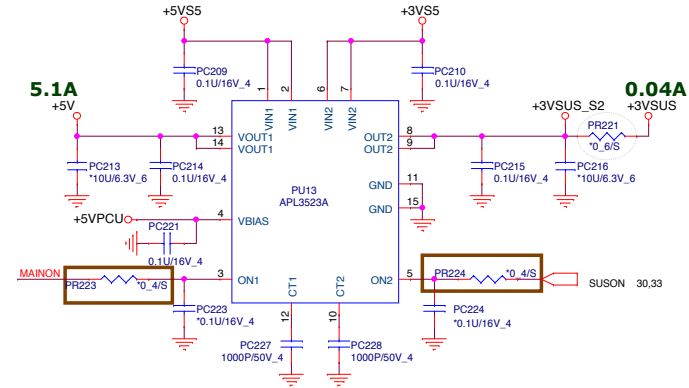
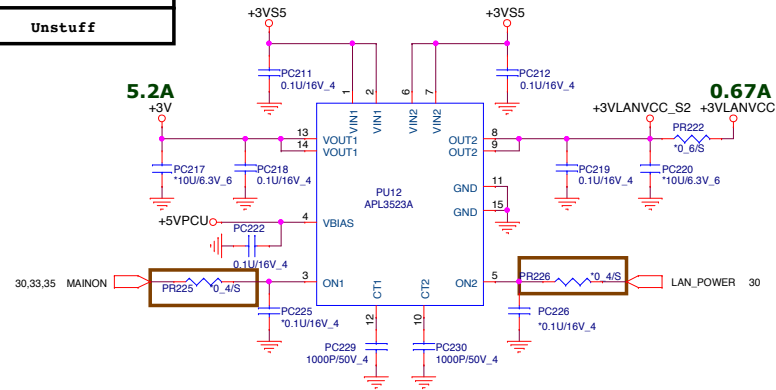




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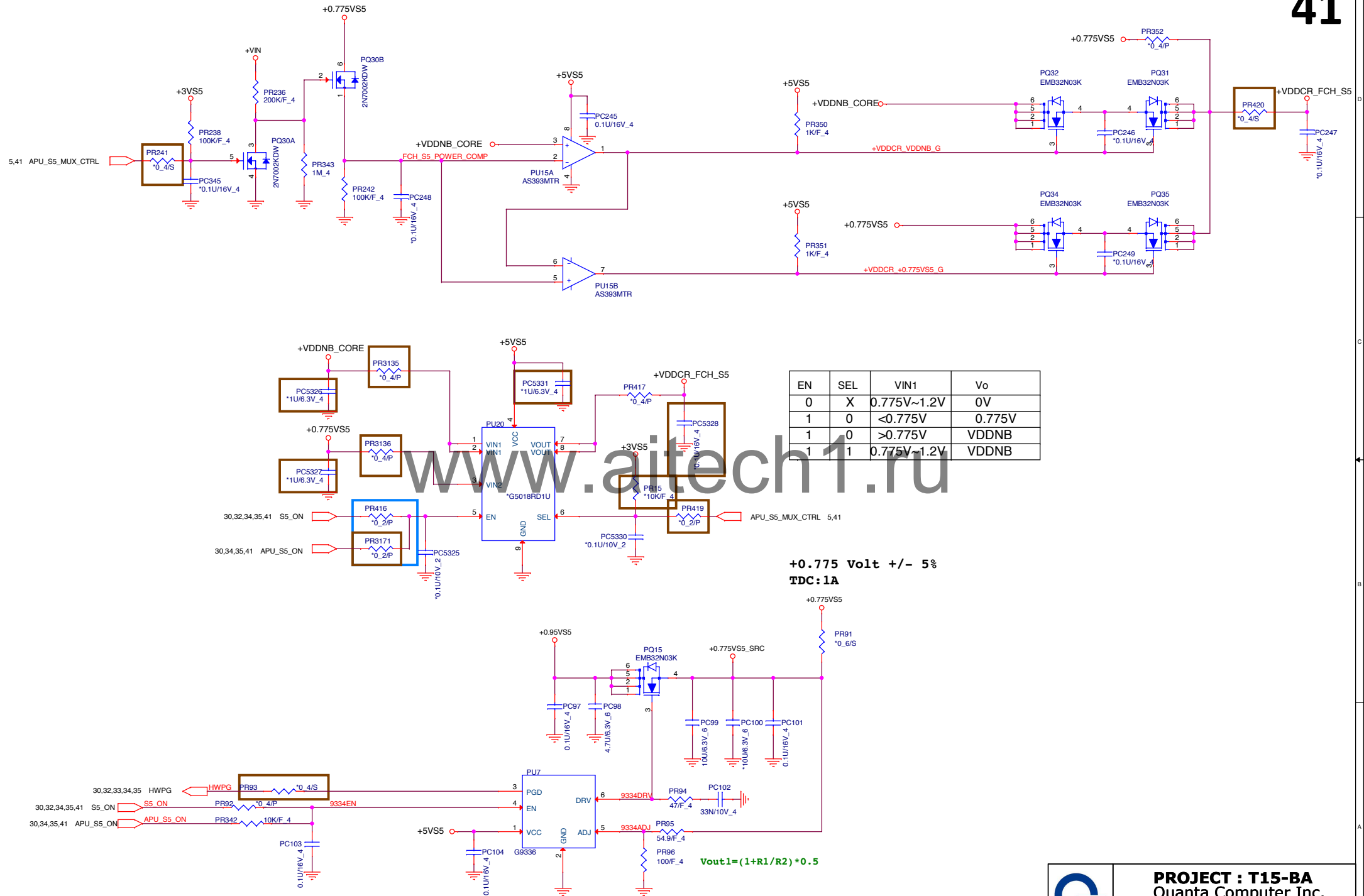


UMA only	Stuff
discrete	Unstuff



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Quanta Computer Inc.

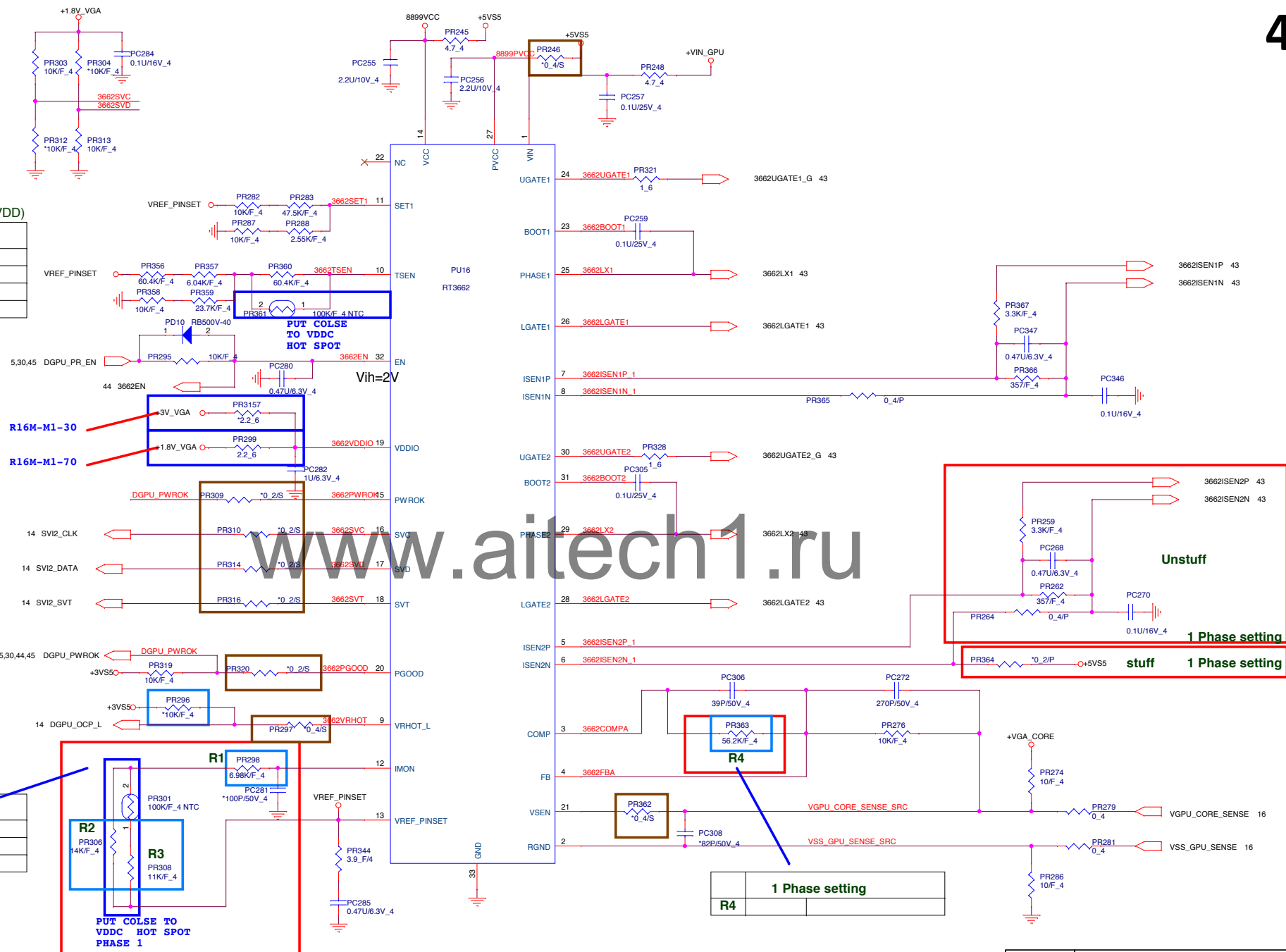
Size Custom	Document Number Load switch IC (APL3523A)	Rev 1A
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Quanta Computer Inc.

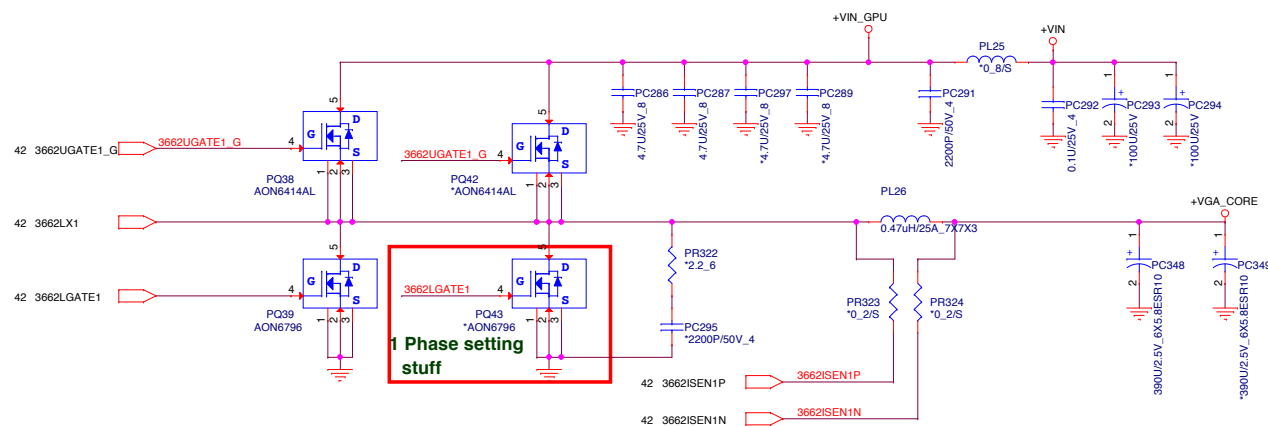
VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

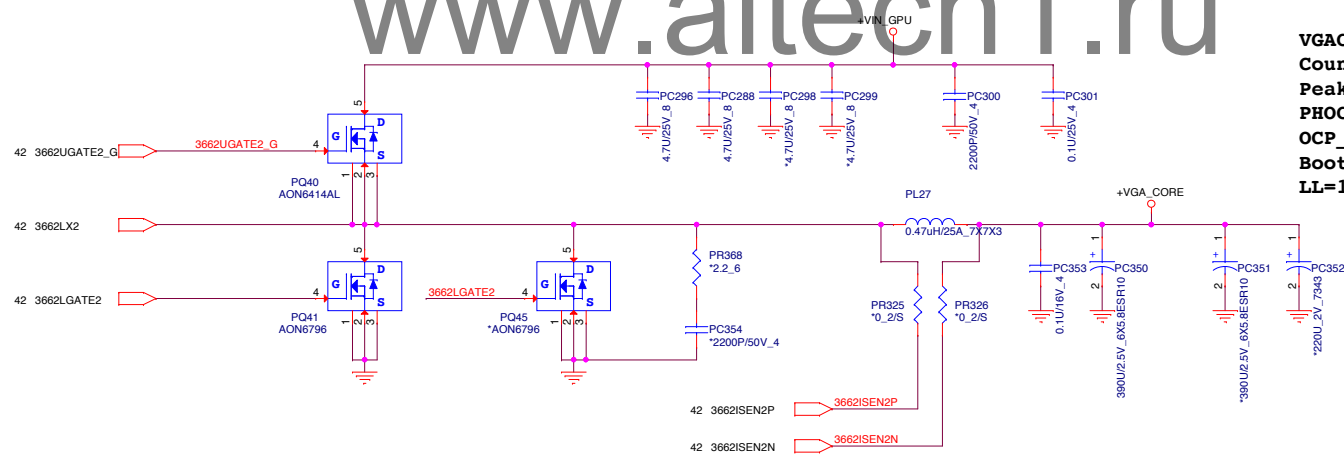


	1 Phase setting	
R1		
R2		
R3		

	1 Phase setting	
R4		



VGACORE (R16M-M1-70_25W/38W(1ms))
 Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=1m V/A



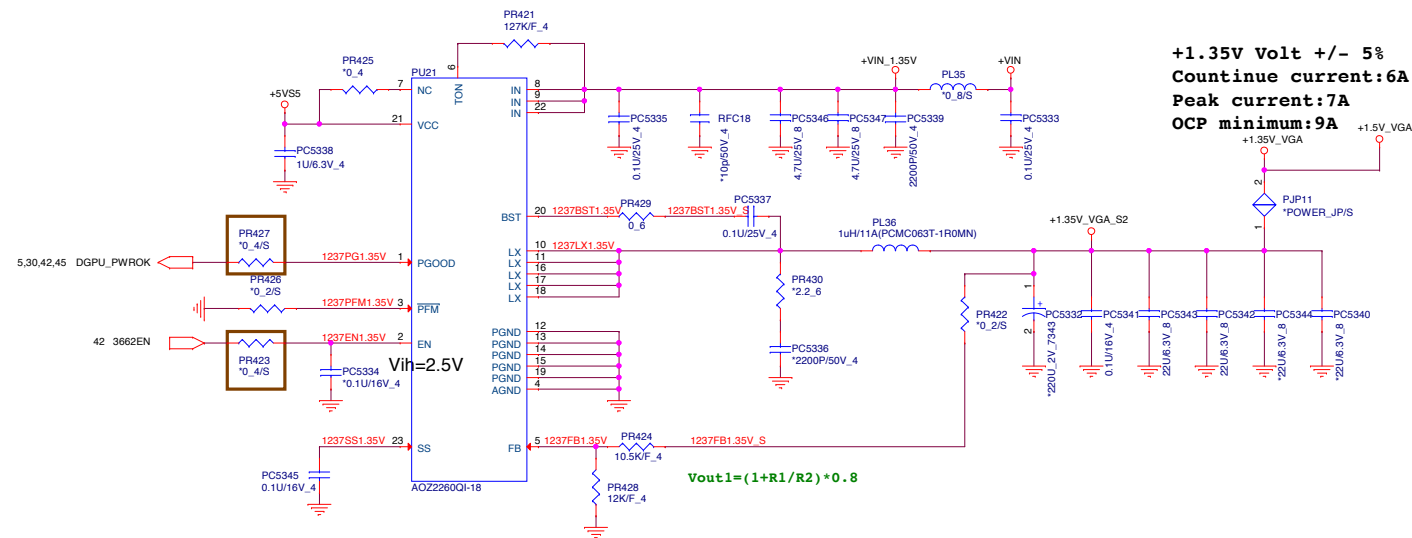
VGACORE (R16M-M2-50_37W/56W(1ms))
 Countinue current:40A (R16M-M2-50)
 Peak current:56A (1mS) (R16M-M2-50)
 PHOCP_TDC=40A
 OCP_SPIKE=75A(1ms)
 Boot VID=0.9V
 LL=1m V/A

Unstuff
 1 Phase setting

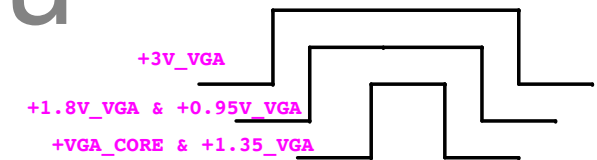
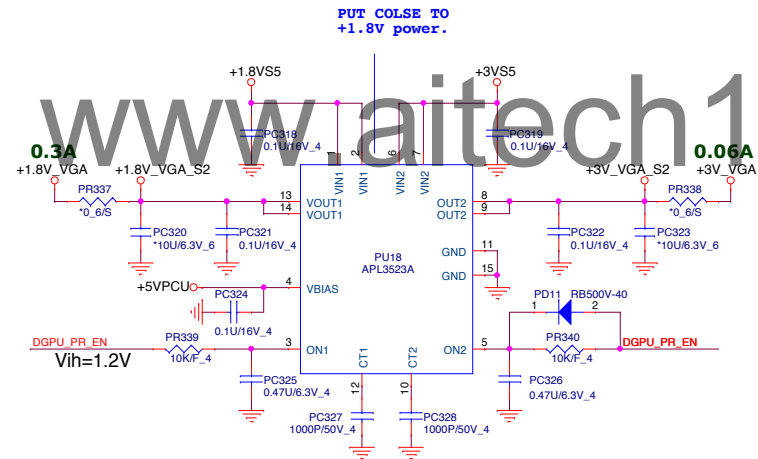
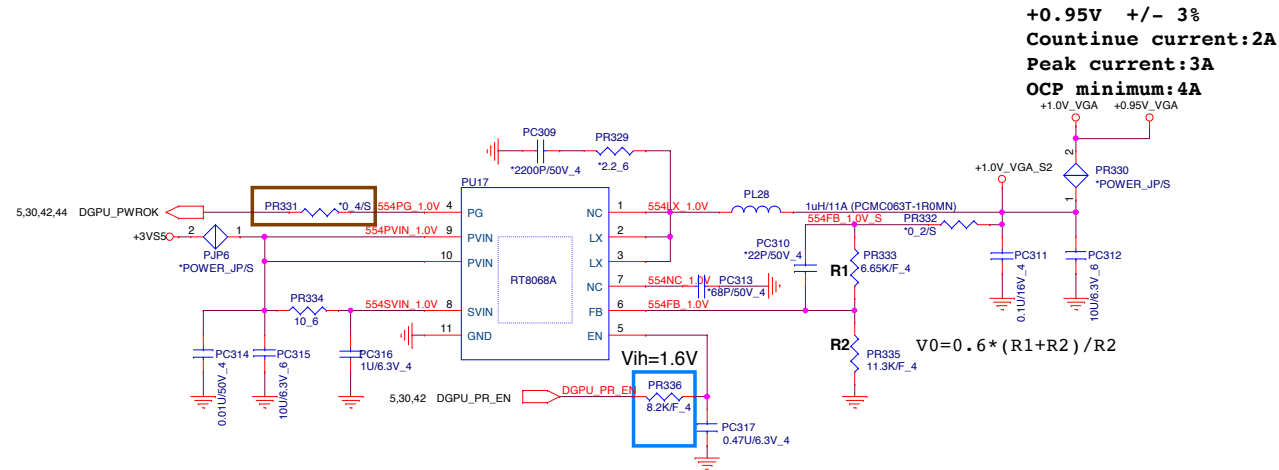


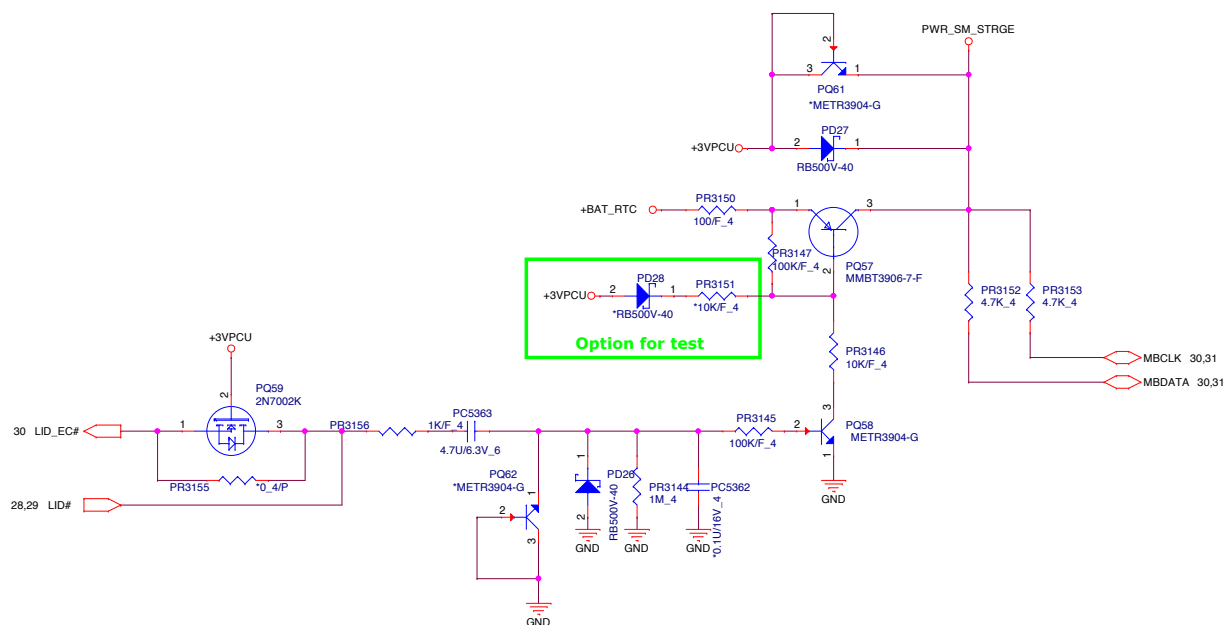
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 Quanta Computer Inc.

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	VGACORE(RT3662EB2)	1A
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